# Synchronous Counter

## What makes a synchronous counter different from an asynchronous (ripple) counter?

- ✓ In a synchronous counter the *same clock pulse* is applied simultaneously to the clock input of every flip-flop.
- ✓ In a ripple (asynchronous) counter the flip-flops are clocked in succession: one flip-flop's output becomes the clock for the next, producing a ripple of transitions.
- ✓ In synchronous designs the decision to toggle a flip-flop is based on its data/excitation inputs (e.g., T or J/K) *at the instant of the clock edge*.
    - For a T flip-flop: if T = 0 → no change; if T = 1 → complement.
    - For a JK flip-flop: if J = K = 0 → no change; if J = K = 1 → complement.

**What are the Key properties of synchronous counters?**

- All flip-flops share the same clock (no ripple propagation), so no ripple-settling time is required.
- Next states are computed from current outputs using combinational logic, not from chained clocking.
- They usually require more combinational gates than ripple counters, but they are faster and more predictable.
- Design involves deriving input equations (T, J/K, or D) from present-to-next-state relationships (often using K-maps).

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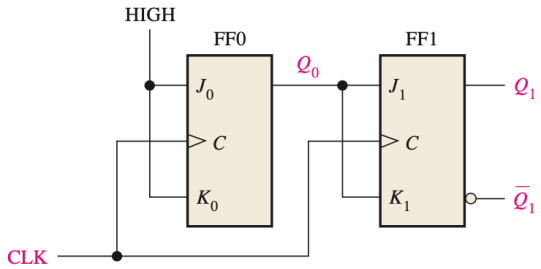
**What are the Recommended design steps?**

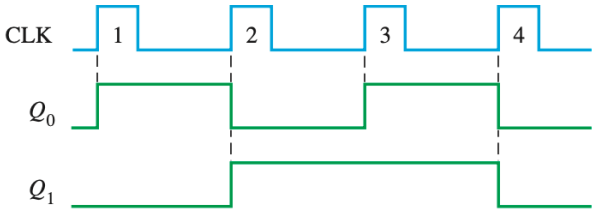
- Determine the number of flip-flops n for the required modulus N: choose the smallest n with $2^n \geq N$.
- Draw the state diagram/list present states → next states.
- Make the flip-flop excitation table (for T, JK or D) and the state transition table.
- For each flip-flop, form the Boolean expression for the required input (T, J/K, or D) that will cause the present → next transition.
- Simplify using K-maps and implement the combinational logic.
- Draw final circuit and verify timing/edge cases (resets, unused states).

## Synchronous Counter

**Ex1: Design a 2-bit Synchronous Up Counter using (JK flip-flop) and draw the Waveform Timing Diagram**

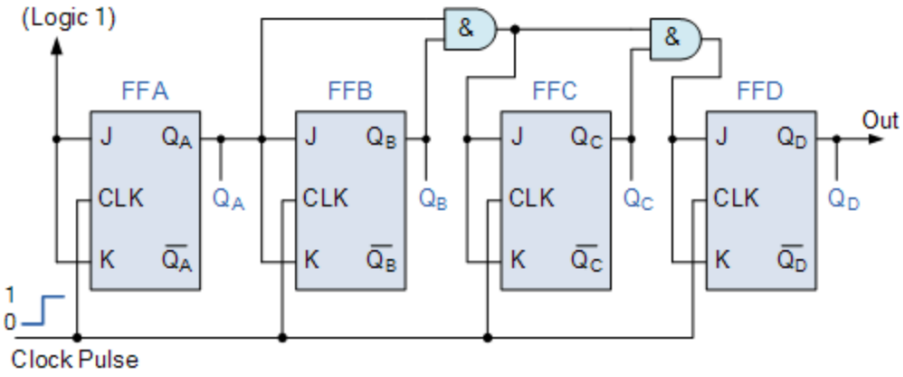



2-Bit Synchronous Binary Counter

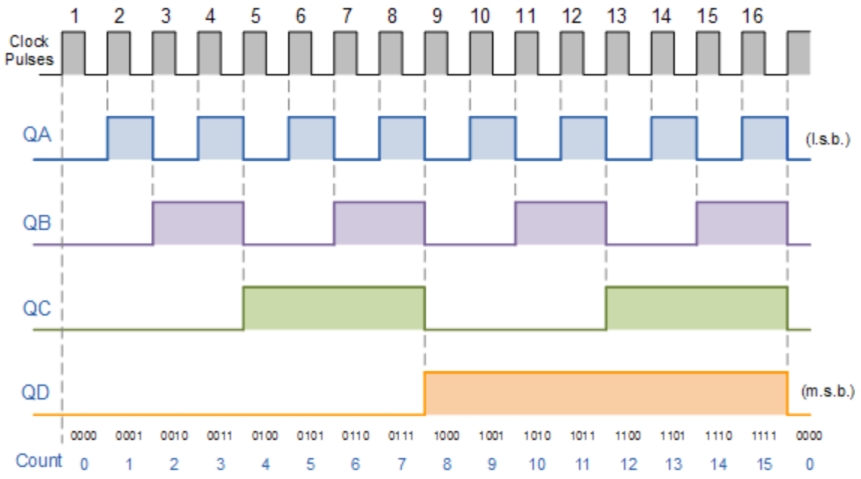



Waveform Timing Diagram

**Ex2: Design a 4-bit Synchronous Up Counter using (JK flip-flop) using AND gate as a control element, and draw the Waveform Timing Diagram**




The J and K inputs of flip-flop FFB are connected directly to the output $Q_A$ of flip-flop FFA, but the J and K inputs of flip-flops FFC and FFD are driven from separate AND gates which are also supplied with signals from the input and output of the previous stage. These additional AND gates generate the required logic for the JK inputs of the next stage. Because this 4-bit synchronous counter counts sequentially on every clock pulse the resulting outputs count upwards from 0 ( 0000 ) to 15 ( 1111 ).

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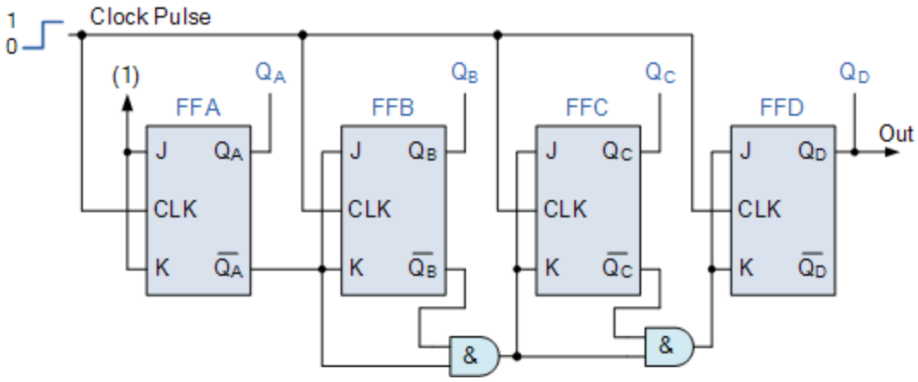
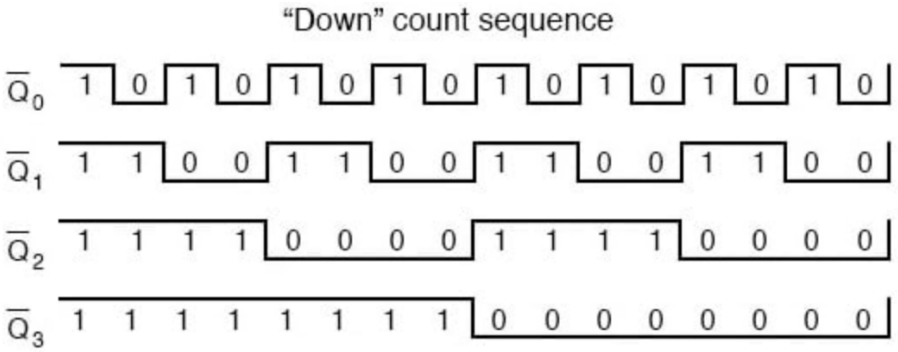
**A 4-bit Synchronous Down Counter can easily** construct by connecting the AND gates to the Q output of the flip-flops, as shown to produce a waveform timing diagram, the reverse of the Ex1. Here, the counter starts with all of its outputs HIGH ( 1111 ) and it counts down on the application of each clock pulse to zero ( 0000 ) before repeating again.




Because this 4-bit synchronous counter counts sequentially on every clock pulse the resulting outputs count downwards from 15 ( 1111 ) to 0 ( 0000 ).

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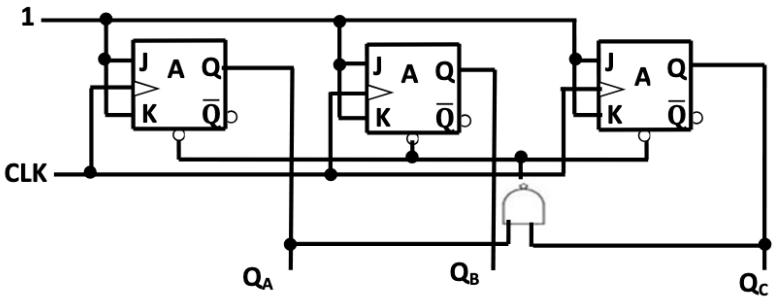
**Ex3 / Design Mod (6) (JK) up Synchronous Counter using a NAND gate as a control element**




| C | B | A | COUNT |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 5 |
| 0 | 0 | 0 | 0 |

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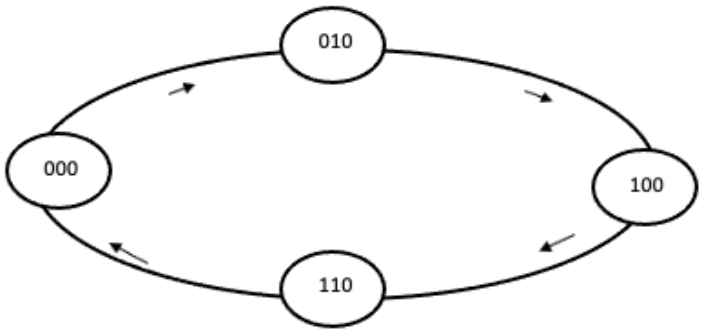
## Lab work:

**Lab1/ Design (3bits) counter, that counts only, even numbers using *T* flip-flops with negative edge clock pulse.**

Sol: the excitation table of ***T*** flip-flop is

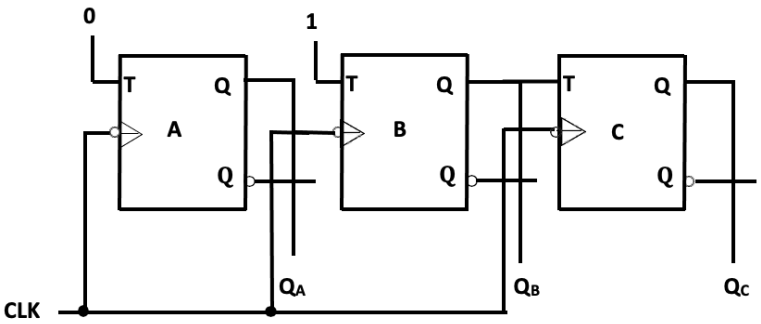
| $Q_t$ | $Q_{t+1}$ | T |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

State Diagram:




| C | B | A | $T_A$ | $T_B$ | $T_C$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 |

Now T inputs of each flip-flop can be found from the following table :

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## Assignment 1:

Design a synchronous up counter using D flip flops that goes through states 0, 1, 2, 4, 0. The unused states must always go to zero on the next clock pulse.

المطلوب:

Step 1 − Number of flip flops required

Step 2 − Draw the state diagram

Step 3 − Choose the type of flip-flop and write the excitation table.

Step 4 − Derive the minimal expression

Step 5 − Draw the logic circuit diagram

## Homework1:

Design 3 bits synchronous up/ down counter using JK flip-flop

Step 1 − Number of flip flops required

Step 2 − Draw the state diagram

Step 3 − Choose the type of flip-flop and write the excitation table.

Step 4 − Draw the logic circuit diagram

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