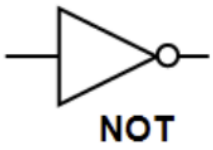
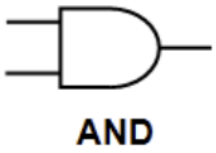
Introduction to logic gates:



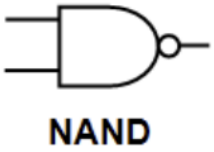
NOT

Input	Output
I	F
0	1
1	0



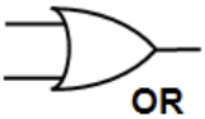
AND

Inputs		Output
A	B	F
0	0	0
1	0	0
0	1	0
1	1	1



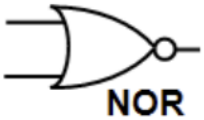
NAND

Inputs		Output
A	B	F
0	0	1
1	0	1
0	1	1
1	1	0



OR

Inputs		Output
A	B	F
0	0	0
1	0	1
0	1	1
1	1	1



NOR

Inputs		Output
A	B	F
0	0	1
1	0	0
0	1	0
1	1	0

EXCLUSIVE OR

Inputs		Output
A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

EXCLUSIVE NOR

Inputs		Output
A	B	F
0	0	1
0	1	0
1	0	0
1	1	1

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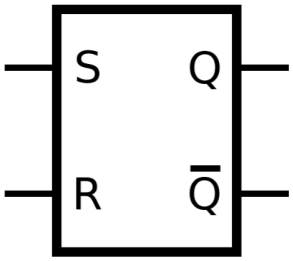
The SR Latch

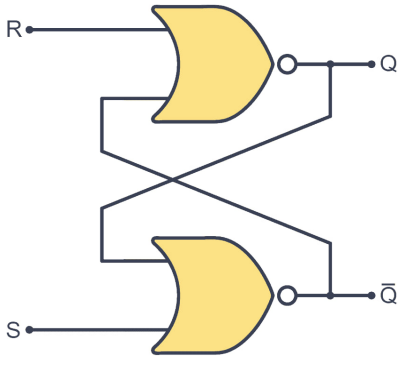
The **SR Latch**, also known as the **Set-Reset Latch**, is a fundamental digital memory circuit that stores one bit of binary data using two inputs, namely Set (S) and Reset (R). When Set is activated, the latch outputs '1' (HIGH), and when Reset is activated, it outputs '0' (LOW). The stored value remains stable even after inputs are removed, making it a **basic memory element**. This latch can be built using either NOR or NAND gates, with the key difference being that NAND implementation uses inverted (active LOW) inputs compared to NOR gates.



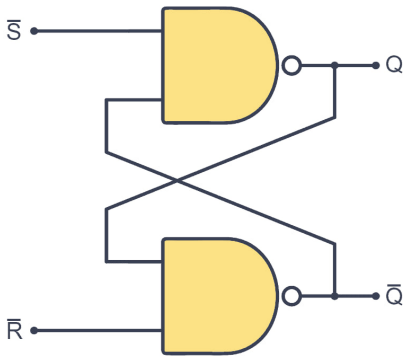
S-R Latch Symbol

Key Elements of SR Latches

- **Set (S) Input:** Forces Q output to the HIGH state (logic 1)
- **Reset (R) Input:** Forces Q output to the LOW state (logic 0)
- **Q Output:** Primary output (representing stored bit)



SR Latch NOR Gate



SR Latch NAND Gat

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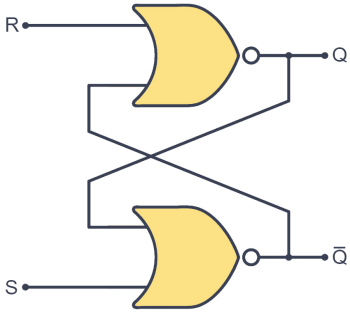
NOR-Based SR Latch Truth Table



S	R	Q	Q'	State
0	0	Q	Q'	Hold (No Change)
0	1	0	1	Reset
1	0	1	0	Set
1	1	0	0	Invalid (Avoided)

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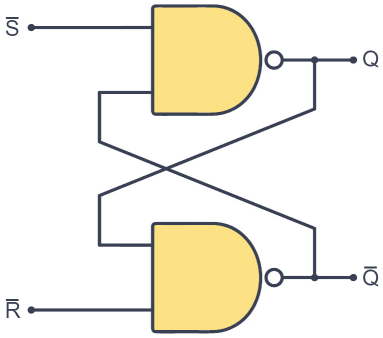
NAND-Based SR Latch Truth Table



S'	R'	Q	Q'	State
1	1	Q	Q'	Hold (No Change)
1	0	0	1	Reset
0	1	1	0	Set
0	0	1	1	Invalid (Avoided)

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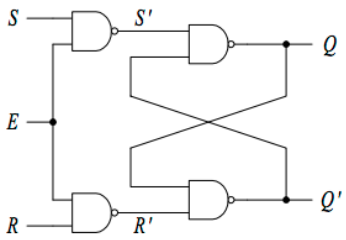
Homework:

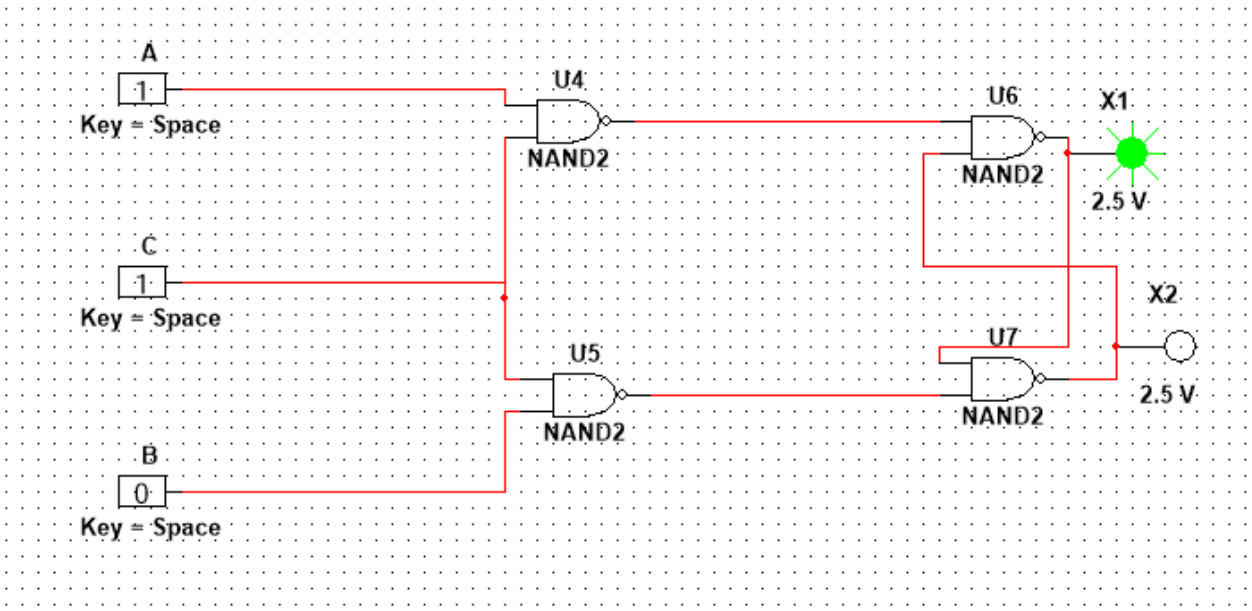
1- Design an electronic circuit in Multisim with three inputs (A, B, C) using the SR latch approach with only four NAND gates, TRUTH TABLE.



(a)

E	S	R	Q	Q_{next}	Q_{next}'
0	×	×	0	0	1
0	×	×	1	1	0
1	0	0	0	0	1
1	0	0	1	1	0
1	0	1	×	0	1
1	1	0	×	1	0
1	1	1	×	1	1

(b)



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