Asynchronous up/ down binary counter

The flip-flops are the fundamental logic elements used to build counter circuits because they can store information, meaning that the previous output can affect the present output. By connecting flip-flops in specific ways, different types of counters can be designed.

The number of flip-flops used and the way they are connected determine the number of possible states (called the modulus (MOD)) and the specific sequence of states that the counter follows during each complete cycle.

For example, a binary mod-8 counter has eight counting states, ranging from 000_2 to 111_2, which means it actually counts from 0 to 7 .

- Modulus (MOD) – the number of states it counts in a complete cycle before it goes back to the initial state.
- Thus, the number of flip-flops used depends on the MOD of the counter (ie; MOD-4 use 2 FF (2-bit), MOD-8 use 3 FF (3-bit), etc..)
- Example: MOD-4 Ripple/Asynchronous Up-Counter

Counters are mainly used in **counting applications**, such as measuring the **time interval** between two unknown instants or measuring the **frequency** of a given signal.

Counters are generally classified into **two main types**:

- Asynchronous counters
  - ❖ The clock signal (CLK) is only used to clock the first FF.
  - ❖ Each FF (except the first FF) is clocked by the preceding FF.
- Synchronous counters

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- ❖ The clock signal (CLK) is applied to all FF, which means that all FF share the same clock signal; thus, the output will change at the same time.

The design steps of sequential counters:

1. The **number of flip-flops** required is equal to the number of bits needed to represent the desired states.
2. All flip-flops must operate in the **toggle mode**.
3. For **up-counters**, the **inverted output ($\bar{Q}$)** of the first flip-flop is used as the clock input for the next flip-flop, and so on, when the flip-flops are triggered by the **positive edge** of the clock pulse.
4. For **down-counters**, the **non-inverted output (Q)** of the first flip-flop is used as the clock input for the next flip-flop, and so on, when the flip-flops are triggered by the **positive edge** of the clock pulse.

- ✓ When the flip-flops are triggered by the **negative edge** of the clock pulse, the **third and fourth conditions** are reversed.

Asynchronous Counter

An **asynchronous counter**, also called a **ripple counter** or **serial counter**, is made of flip-flops connected in a series. The **clock** is applied only to the first flip-flop, and each subsequent flip-flop receives its clock input from the output of the previous one. The number of flip-flops determines the **modulus** (total count before repeating).

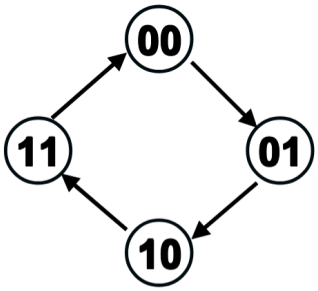
These counters can be used as **up-counters** or **down-counters** and have the following characteristics:

- ❑ Simple in design.
- ❑ Require minimal hardware.

- Flip-flops are triggered one after another.
- Counting operation "ripples" through the flip-flops, making them relatively slow compared to synchronous counters.

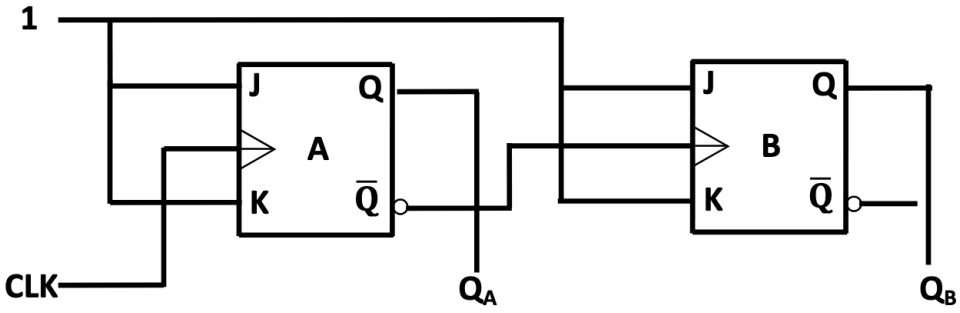
The Asynchronous Counter that counts 4 number starts from 00 -> 01 -> 10 -> 11 and back to 00 is called MOD-4 Ripple (Asynchronous) Up-Counter.

Present State	Next State
Q_1Q_0	Q_1Q_0
00	01
01	10
10	11
11	00



Example 1: Design up asynchronous counter has the following sequence (00, 01, 10, and 11) using J-K flip-flops with a positive edge clock pulse.

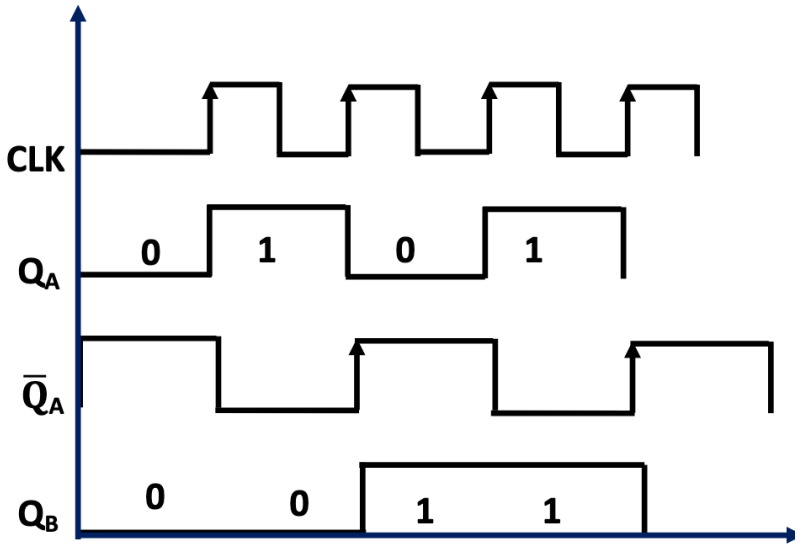
Answer:



Example 2: For the circuit shown in example (1), draw the timing diagram and truth table.

Answer:

B	A	Output
0	0	0
0	1	1
1	0	2
1	1	3



Homework 1: Design (3-bits) up counter using J-K flip-flops with a positive edge clock pulse.

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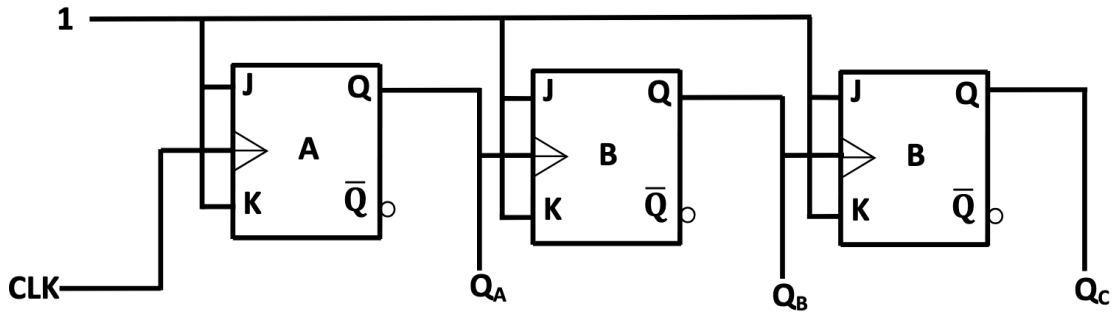
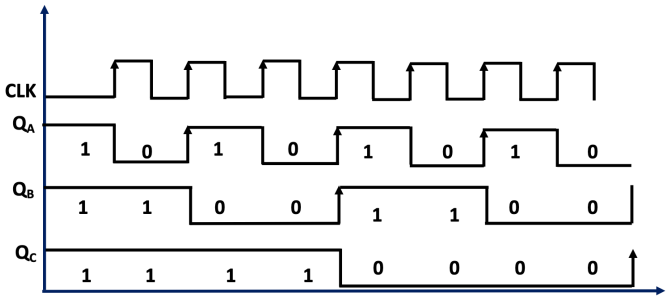
Example 3: Design (3-bits) down counter using J-K flip-flops with positive edge clock pulse and draw the timing diagram and truth table of the counter.

Answer:





C	B	A	Output
1	1	1	7
1	1	0	6
1	0	1	5
1	0	0	4
0	1	1	3
0	1	0	2
0	0	1	1
0	0	0	0

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HomeWorks:

HW2: design a (3-bits) up counter using T flip-flops with negative edge clock pulse, draw the timing diagram and truth table for this counter.

HW3: design a (4-bits) up counter using D flip-flops with negative edge clock pulse, draw the timing diagram and truth table for this counter.

HW4: design a (2-bits) down counter using D flip-flops with negative edge clock pulse, draw the timing diagram and truth table for this counter.

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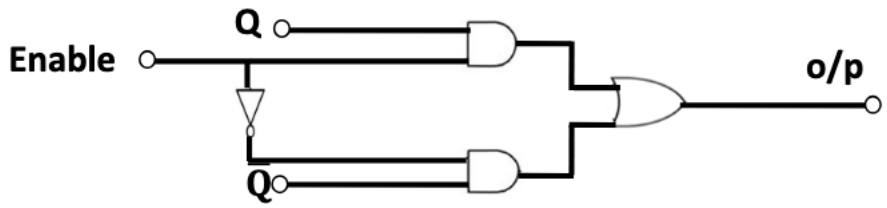
Homework: Until 11:58 PM 28/10/2025

Design (4-bits) up-down counter using J-K flip-flops with positive edge clock pulse and draw the timing diagram and truth table for this counter.

Important Note: to design up-down counter at the same time, enable element can be used with the circuit shown below



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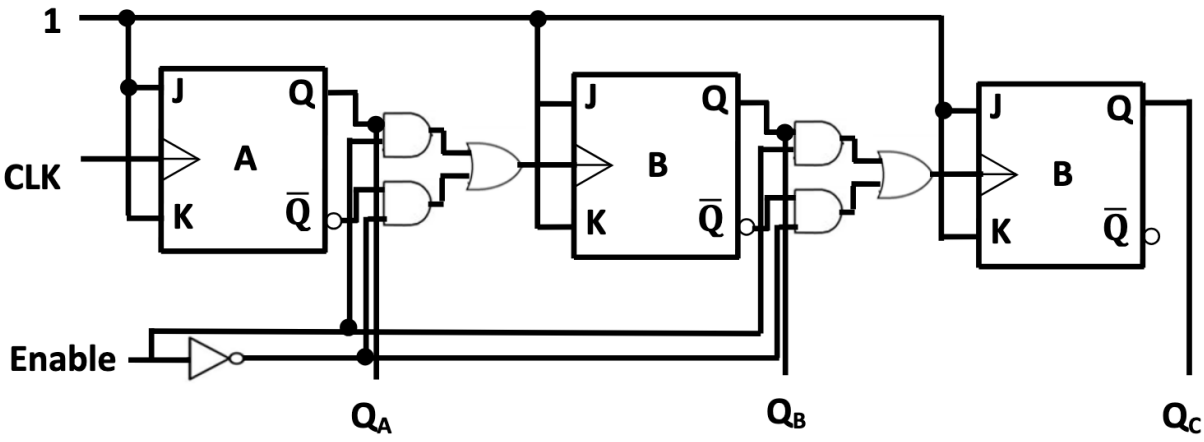

(4-bits) up-down counter using J-K flip-flops

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