Flip-Flops

Flip-flops are synchronous bistable devices, also known as bistable multivibrators. In this case, the term synchronous means that the output changes state only at a specified point (leading or trailing edge) on the triggering input called the clock (CLK), which is designated as a control input, C; that is, changes in the output occur in synchronisation with the clock.

Flip-flops are edge-triggered or edge-sensitive, whereas gated latches are level-sensitive.
A flip-flop is a bistable digital circuit that can store one bit of information—either logic 0 or 1.

Figure 1 The S and R in SR flip-flop mean 'SET' and 'RESET' respectively.

Types Of Flip-flops

There are different types of flip-flops depending on how their inputs and clock pulses cause transition between two states. We will discuss different types of flip-flops such as: S-R, D, J-K, T and Master-Slave. Basically D, J- K, and T are three different modifications of the S-R flip-flop.

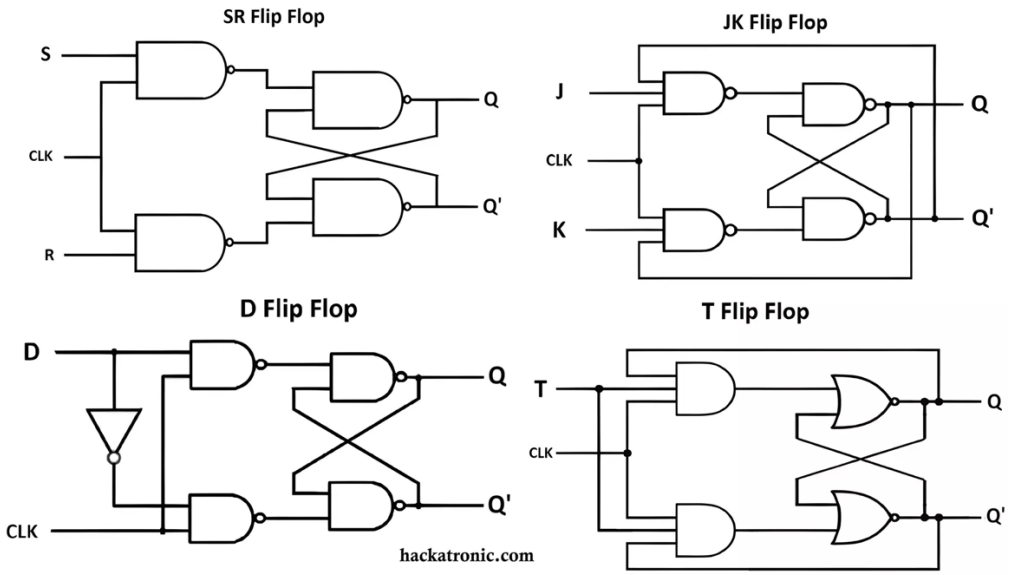


Figure 2 Types of Flip-Flops

SR Flip-Flops

SR flip-flop is one of the fundamental parts of the sequential circuit.

The SR is a flip-flop with two inputs, one is S and the other is R. S here stands for Set and R here stands for Reset. The set basically indicates set the flip flop, which means output 1 and the reset indicates resetting the flip flop, which means output 0. Here, a clock pulse is supplied to operate this flip-flop; hence it is a clocked flip-flop.

The symbolic representation of the SR Flip Flop is shown below:

Figure 3 The S and R in SR flip-flop mean 'SET' and 'RESET' respectively.

SR Flip-Flop working principle

SR flip-flop works during the transition of clock pulse either from low to high or from high to low (depending on the design), i.e. it can be either positive edge triggered or negative edge triggered.

For a positive-edge triggered SR flip-flop, suppose, if S input is at high level (logic 1) and R input is at low level (logic 0) during a low to high transition on clock pulse, then the SR flip-flop is said to be in SET state and the output of the SR flip-flop is SET to 1.

For the same clock situation, if the R input is at high level (logic 1) and S input is at low level (logic 0), then the SR flip-flop is said to be in RESET state and the output of the SR flip-flop is RESET to 0.

SR Flip Flop

Generally, synchronous circuits change their states only when clock pulses are present. The operation of the basic flip-flop can be modified by including an additional input to control the behaviour of the circuit.

When a clock pulse is used as the control signal, the inputs R and S may be clocked (entered) into the flip-flop by a set of NAND gates. Such a circuit is shown below: -

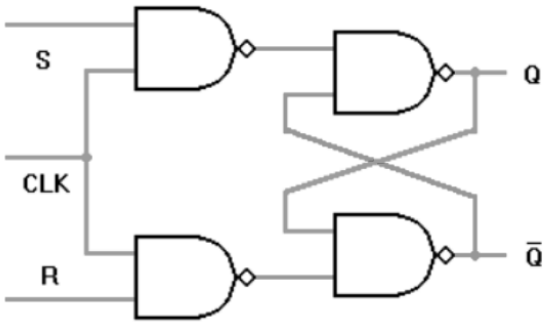
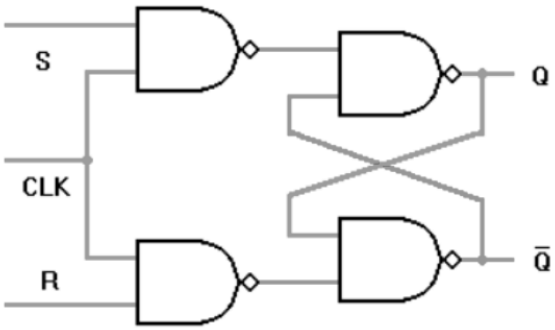


Figure 4 SR Flip Flop with four NAND gates

The circuit shown below consists of four NAND gates. The clock input is connected to both of the NAND gates. The obvious advantage of this clocked SR flip-flop is that the inputs R and S are considered only when the clock pulse is high. As before, the condition R = S = 1 is invalid and should be avoided.



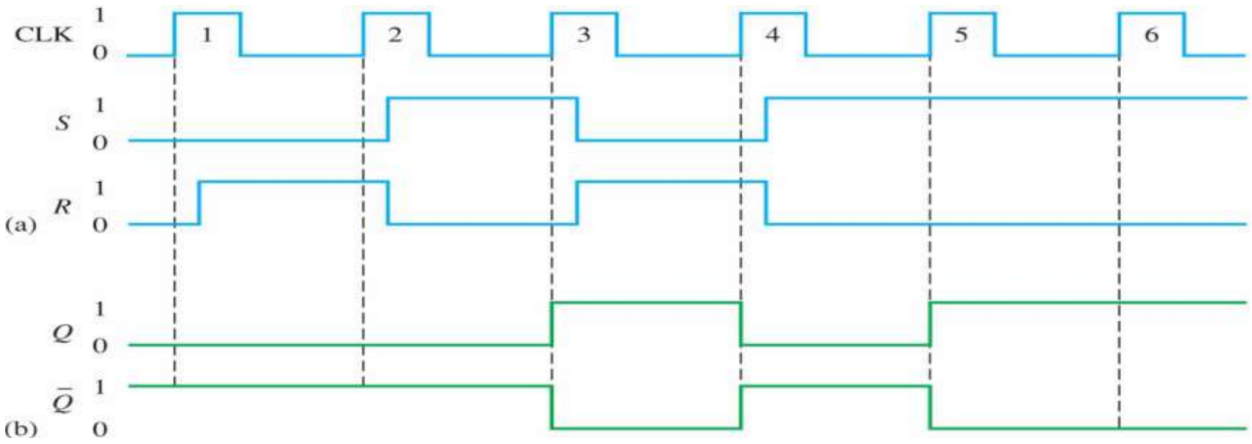
Trigger	Inputs		Output				State
			Present State		Next State		
CLK	S	R	Q	Q'	Q	Q'	
⊠	x	x	-		-		No Change
⊓	0	0	0	1	0	1	No Change
			1	0	1	0	
⊓	0	1	0	1	0	1	Reset
			1	0	0	1	
⊓	1	0	0	1	1	0	Set
			1	0	1	0	
⊓	1	1	0	1	-	-	Indeterminate
			1	0	-	-	

Example: Determine the output waveforms of the flip-flop for the S, R and CLK inputs, assuming that the positive edge-triggered flip-flop is initially RESET.

Truth Table

S	R	Q	$\overline{Q}$
0	0	No change	
0	1	0	1
1	0	1	0
1	1	X (Invalid)	X

The waveforms of the flip-flop:



Applications of SR Flip Flop

There are numerous applications of SR Flip Flop in Digital System, which are listed below:

- **Register:** SR Flip Flop used to create register. Designer can create any size of register by combining SR Flip Flops.
- **Counters:** SR Flip Flops used in counters. Counters count the number of events that occurs in a digital system.
- **Memory:** SR Flip Flops used to create memory which are used to store data, when the power is turned off.
- **Synchronous System:** SR Flip Flop are used in synchronous system which are used to synchronize the operation of different component.

D Flip-Flop - Data or Delay Flip-Flop

A D flip-flop is a **synchronous** input because data on the input is transferred to the flip-flop's output only on the triggering edge of the clock pulse. When *D* is HIGH, the *Q* output goes HIGH on the triggering edge of the clock pulse, and the flip-flop is SET. When *D* is LOW, the *Q* output goes LOW on the triggering edge of the clock pulse, and the flip-flop is RESET.

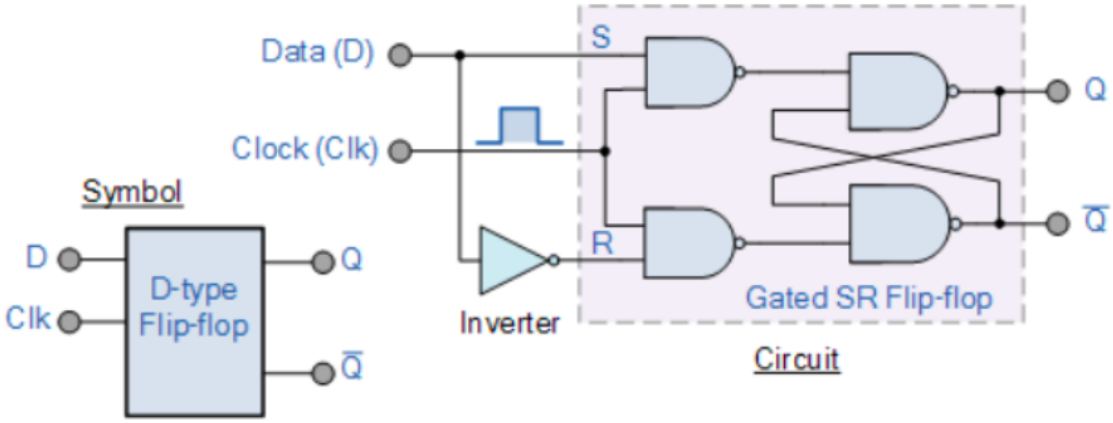
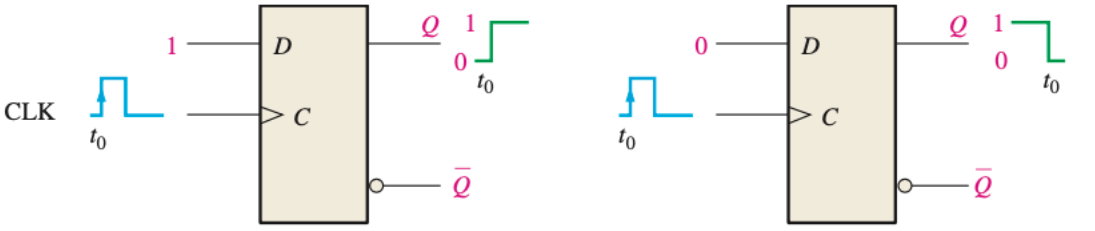


Figure 5 D Flip-Flop

The D-type (Data or delay) flip flop is constructed from a gated SR flip-flop with an inverter added between the S and the R inputs to allow for a single D (Data) input in addition to the clock input as shown in figure above.

This basic operation of a positive edge-triggered D flip-flop is illustrated in Figure 6 (a&b), and Table is the truth table for this type of flip-flop. Remember, *the flip-flop cannot change state except on the triggering edge of a clock pulse.* The *D* input can be changed at any time when the clock input is LOW or HIGH (except for a very short interval around the triggering transition of the clock) without affecting the output. Just remember, *Q* follows *D* at the triggering edge of the clock.



(a) $D = 1$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)

(b) $D = 0$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)

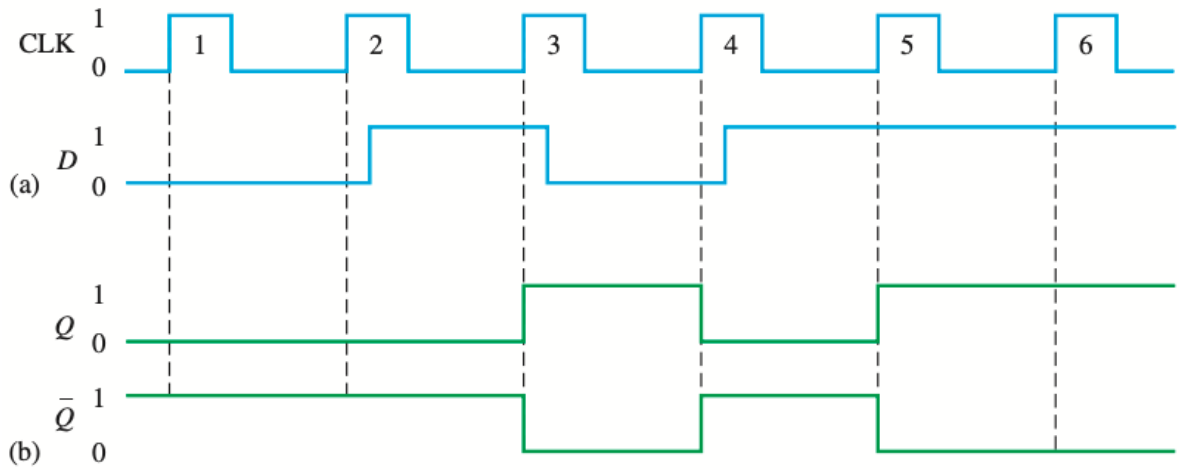
Figure 6 D flip-flop set and reset

Truth table for a positive edge-triggered D flip-flop.

Inputs		Outputs		
D	CLK	*Q*	$\overline{Q}$	Comments
0	↑	0	1	RESET
1	↑	1	0	SET

↑ = clock transition LOW to HIGH

Example: Determine the *Q* and $\overline{Q}$ output waveforms of the D flip-flop from the Figure below for the *D* and CLK inputs. Assume that the positive edge-triggered flip-flop is initially RESET.



Truth table for a positive edge-triggered D flip-flop.

Inputs		Outputs		
D	CLK	*Q*	$\overline{Q}$	Comments
0	↑	0	1	RESET
1	↑	1	0	SET

↑ = clock transition LOW to HIGH

Solution

- **At clock pulse 1, *D* is LOW, so *Q* remains LOW (RESET).**
- **At clock pulse 2, *D* is LOW, so *Q* remains LOW (RESET).**
- **At clock pulse 3, *D* is HIGH, so *Q* goes HIGH (SET).**
- **At clock pulse 4, *D* is LOW, so *Q* goes LOW (RESET).**
- **At clock pulse 5, *D* is HIGH, so *Q* goes HIGH (SET).**
- **At clock pulse 6, *D* is HIGH, so *Q* remains HIGH (SET).**

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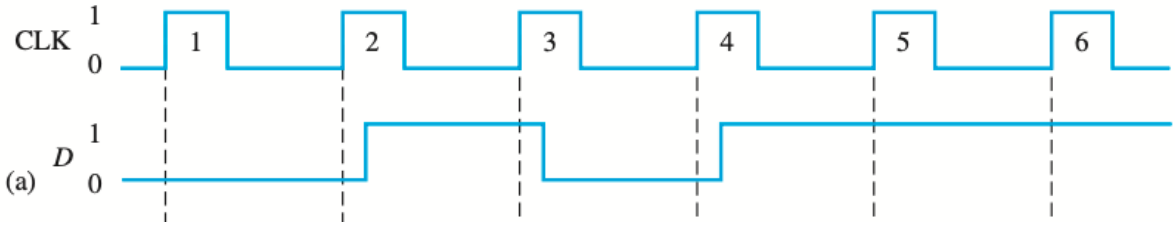
Homework:

Determine the *Q* and $\overline{Q}$ output waveforms of the D flip-flop from the Figure below for the *D* and CLK inputs. Assume that the negative-edge-triggered flip-flop is initially RESET.



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