Al-Mustaqbal University
College of Sciences
Intelligent Medical System Department

Embedded systems

Lecture 5 :

Types of Memories Used In Embedded System

Prof.Dr. Mehdi Ebady Manaa

جامعة المستقبل
AL MUSTAQBAL UNIVERSITY

Types of Memories

- The types of memories are primary and secondary memory. The primary memory will store the data and information until the power supply is present means the memory holds the information only the memory is connected with the power supply. If the power supply goes then the data and information which is stored in the memory will be erased or lost. The primary memories are SRAM and DRAM, later I will discuss what is SRAM and DRAM.
- The secondary memory will store the data and information even if the power supply goes. The data and information will still remain in memory after the power cut. The secondary memories are Flash, EPROM, PROM, Masked ROM, EEPROM, and NVRAM.

Primary memories are used where we want to store temporary data and information and secondary memories are used where we want to store data and information permanently.

Memory Structure

- The memory subsystem is organized as an array of cells or locations
- Each memory location is identified by an address
- The contents of a memory cell is a word
  - A memory word may store instructions or data

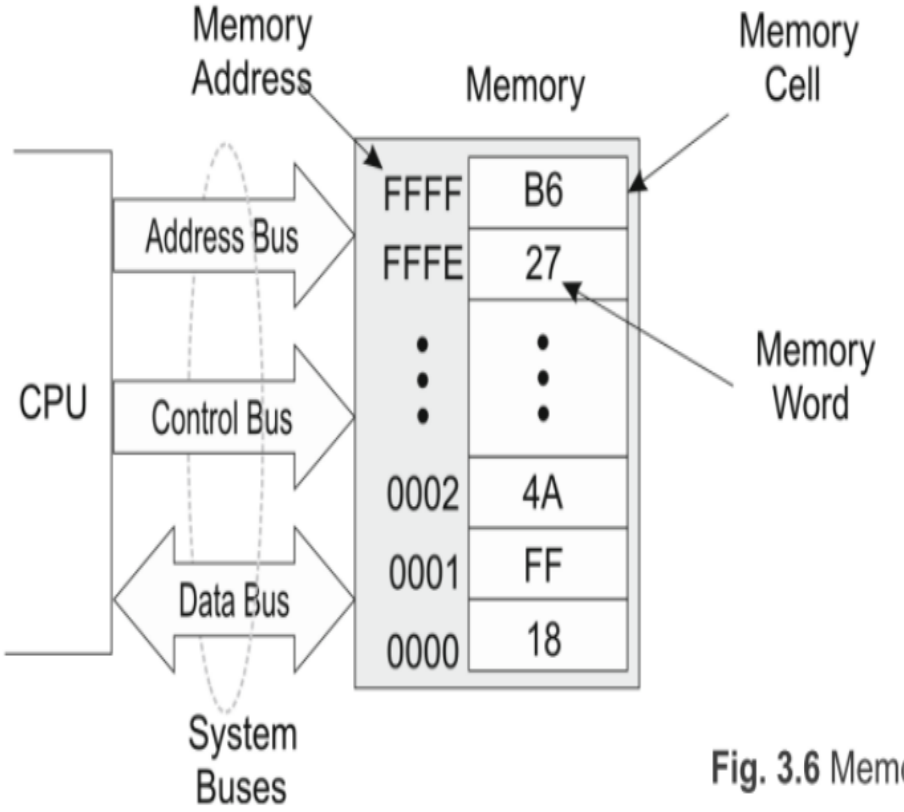
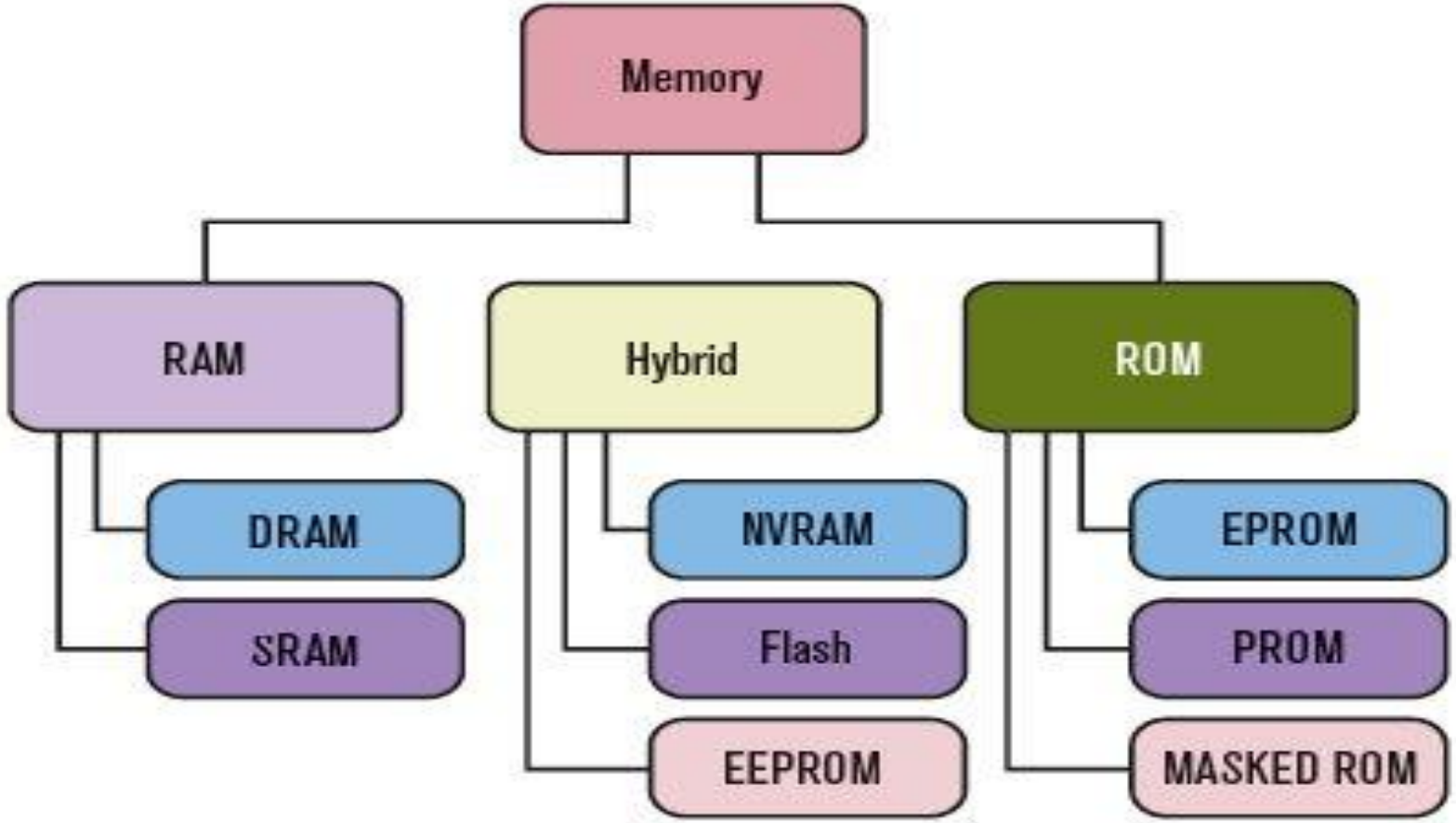


Fig. 3.6 Memory structure

Types of Memories



Common Embedded System Memory Types

Types of Memories

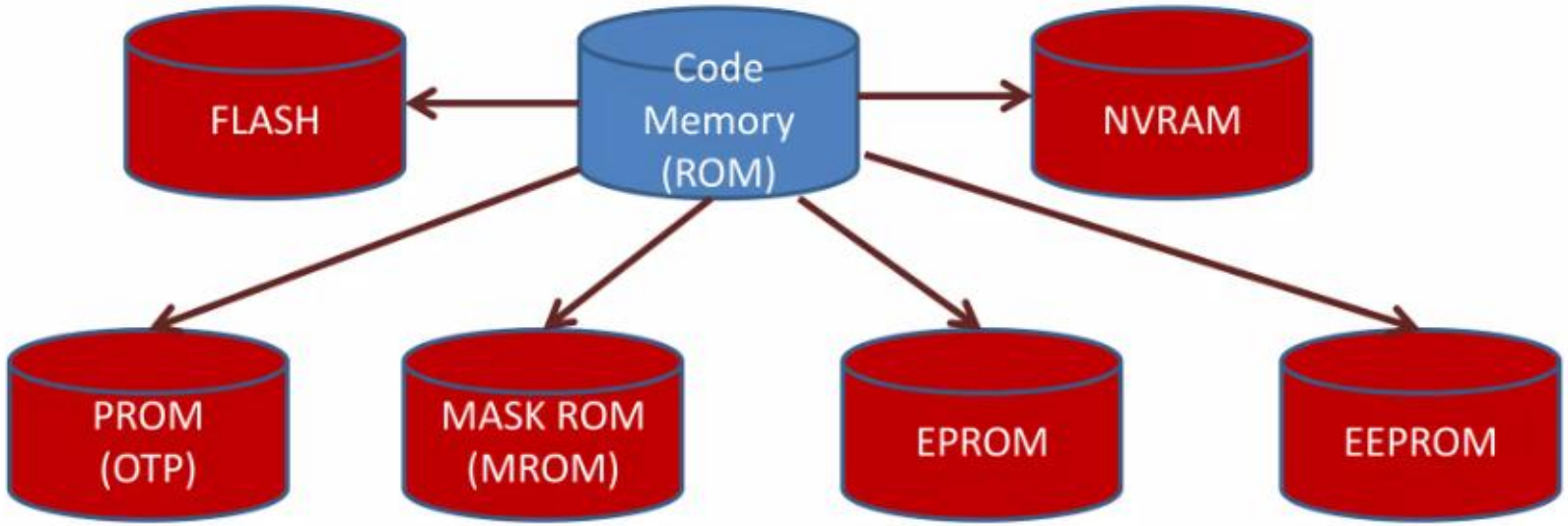
On-Chip Memory and Off-chip Memory

Volatile Memory and Non Volatile Memory

Serial Memory and Parallel Memory

ROM and RAM

Program Storage Memory (ROM):



Types of Memories

Masked ROM

→ One Time Programmable

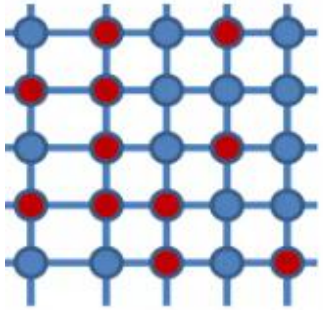
→ Programmed by masking and metallization process at the time of production itself based on input given by user

→ Low cost, good for storing Firmware for low cost embedded devices.

→Once the design is proven and tested, the binary data corresponding to it can be given to MROM Fabricator

→Disadvantage: disability to modify Firmware

PROM



→ One Time Programmable

→ Unlike MROM it is not preprogrammed by manufacturer

→ The end user programs these devices.

→has nichrome/polysilicon arranged as matrix. These wires can be used as fuses.

→it is programmed by selectively burning these fuses according to bit pattern to be stored

→fuses not blown represents '1' and those blown are logic '0'. Default state is logic '1'

→used for commercial production of embedded systems whose prototype is proven and code is finalized.

→low cost is advantage but cannot be reprogrammed

Types of Memories

- **Erasable and Programmable ROM (EPROM)**
- Provides the flexibility to reprogram the same chip
- Stores the bit information by charging the FET gate
- Contains quartz crystal window for erasing the stored information.
- if this window is exposed to UV rays for a fixed duration, the entire memory will be erased
- for erasing process, it needs to be taken out of circuit board and put in a UV eraser device for 20-30 mins, which is tedious and time consuming
- **Electrically Erasable Programmable ROM (EEPROM)**
- Information contained in EEPROM can be altered by electrical signals at register/byte level
- Can be erased and reprogrammed in-circuit
- consists of a 'chip erase mode', in this mode they can be erased in ms.
- provides flexibility for system design
- only limitation is capacity compare to standard ROM

Types of Memories

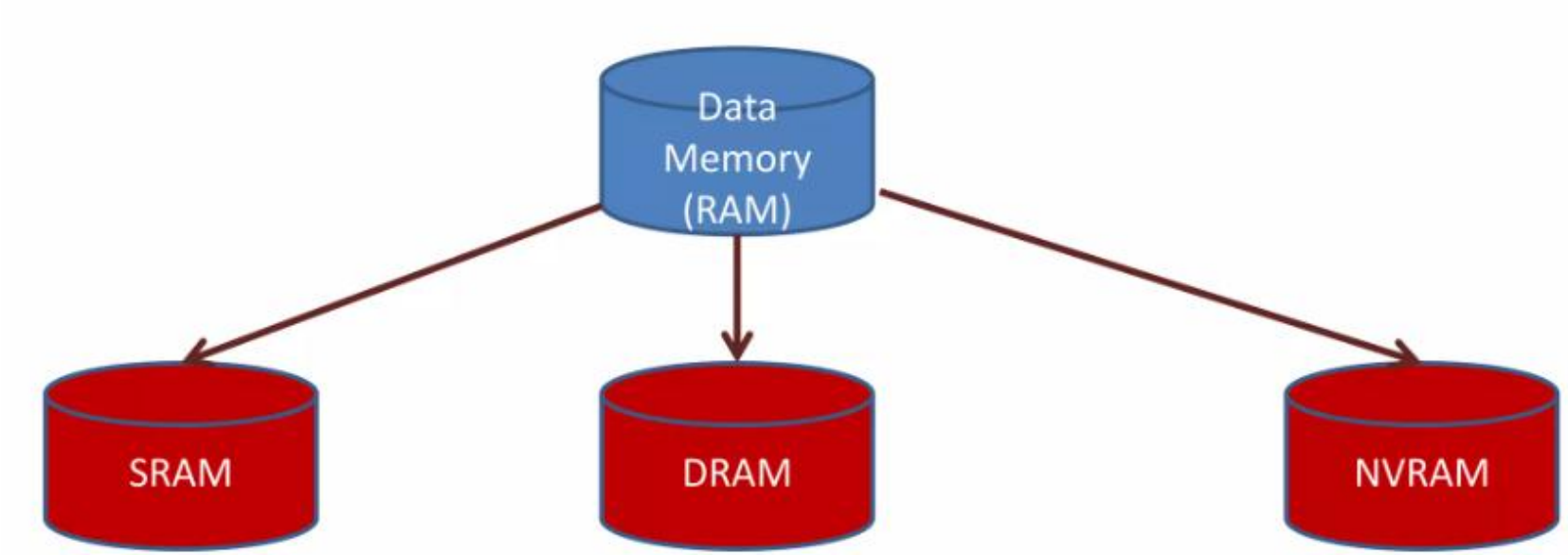
FLASH

- Latest ROM
- Variation of EEPROM
- combines flexibility of EEPROM + High capacity of Standard ROM.
- organized as sectors(blocks) or pages.
- stores information in an array of floating gate MOSFET transistors.
- memory can be erased at sector/page level without erasing other sectors
- each page/sector must be erased before reprogramming, typical erase cycles is 1000 cycles

Non-Volatile RAM (NVRAM)

- Memory with battery back up
- Consists of SRAM memory with minute battery
- Memory and battery are packed in a single package
- life span is expected to be around 10 years

Read/ Write Memory or Random Access Memory (RAM):



Types of Primary Memories

SRAM

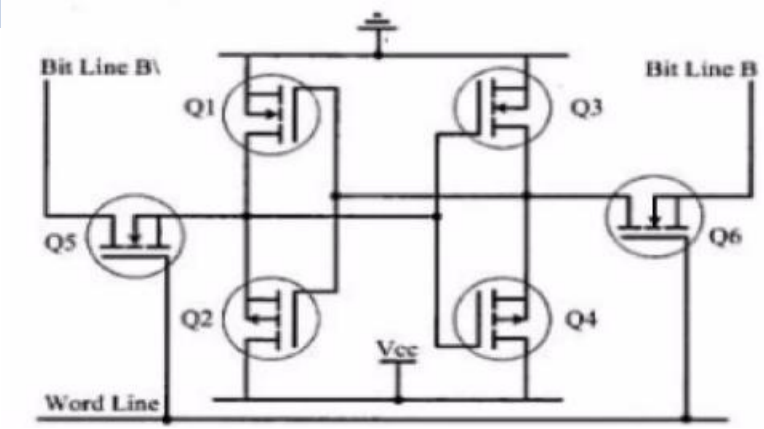
SRAM stands for Static Random Access Memory, this memory consumes less power compared to the DRAM. The static random access memory is 4 times faster than the DRAM. In this memory, data is stored temporarily until the power supply is there. The cost of is memory is high compared to DRAM.

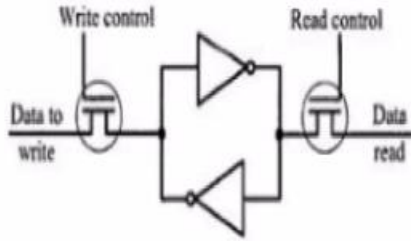
- Data is stored in the form of voltage
- Made up of flip-flops
- Fastest form of RAM
- typically realized using 6 MOSFETS4 for building flip-flops; 2 for controlling access
- in simple form SRAM is a 2 Cross-coupled inverters with read/write control through transistor.
- access to memory cell is controlled by word line
- for writing, desired value is applied to bit line controller. i.e. for 1, B=1 and B'=0

  for 0, B=0 and B'=1
- for reading, both the bit lines are asserted/set as 1 and word line is set to 1

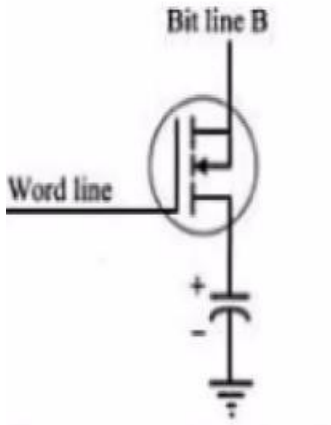
Types of Memories

- **SRAM**





- **Dynamic Random Access Memory (DRAM)**
- Data is stored in the form of charge
- Made up of a MOS transistor gate
- high density and low cost
- Charge gets leaked away hence periodic refresh is done
- DRAM Controller refreshes DRAM after certain msecs.
- MOSFET acts as gate for incoming and outgoing data
- capacitor acts as bit storage unit



SRAM vs. DRAM

SRAM	DRAM
→made up of 6 CMOS transistors (MOSFETs)	→made up of a MOSFET and capacitor
→doesn't require refresh	→periodic refresh is necessary
→low capacity (less dense)	→high capacity
→expensive	→less expensive
→fast in operation, 10 ns access time	→slow in operation due to refreshment 60 ns access time Write is faster than read

Types of Memories

Memory Shadowing

	Advantage	Limitation
ROM	Non Volatile	Slower
RAM	Faster	Volatile

→ ROM access speed is very slow compared to RAM

→ RAM is 3 times faster than ROM

→ Shadowing technique is adapted to solve execution speed problem

→Basic I/P O/P configuration ROM or BIOS stores hardware configuration information like address of various ports.

Now manufactures include RAM behind BIOS at its same address, as a shadow BIOS

→First step during Boot up is copying of BIOS to shadowed RAM and write protecting this RAM and disabling BIOS

→RAM is volatile but ROM is permanent, therefore high system performance is achieved by accessing RAM instead of ROM

Types of Memories

Memory Selection for Embedded System

→Code Memory (ROM)
→ Data Memory (RAM)
} Application Specific

→if made up of Soc/MC, on-chip memory may be enough, if not must be interfaced with external/off-chip memory

→ROM + RAM to execute program code, for RTOS based embedded system extra RAM is required for Memory Shadowing

→Memory Chip Size →available in standard size like 512/1024 bytes (1Kb, 2Kb, 4Kb, 8Kb, 1Gb, 2Gb, 4Gb, 8Gb)
→suppose memory required is 740 bytes, 1Kb chip can be selected

→word size →no. of bits that can be accessed simultaneously, word size <==> bus size

→currently FLASH memory is used

→FLASH memory →NAND FLASH memory →High density, low cost, DRAM is used
→NOR FLASH memory →low density, slightly expensive but supports XIP (execute in place)

Memory Types

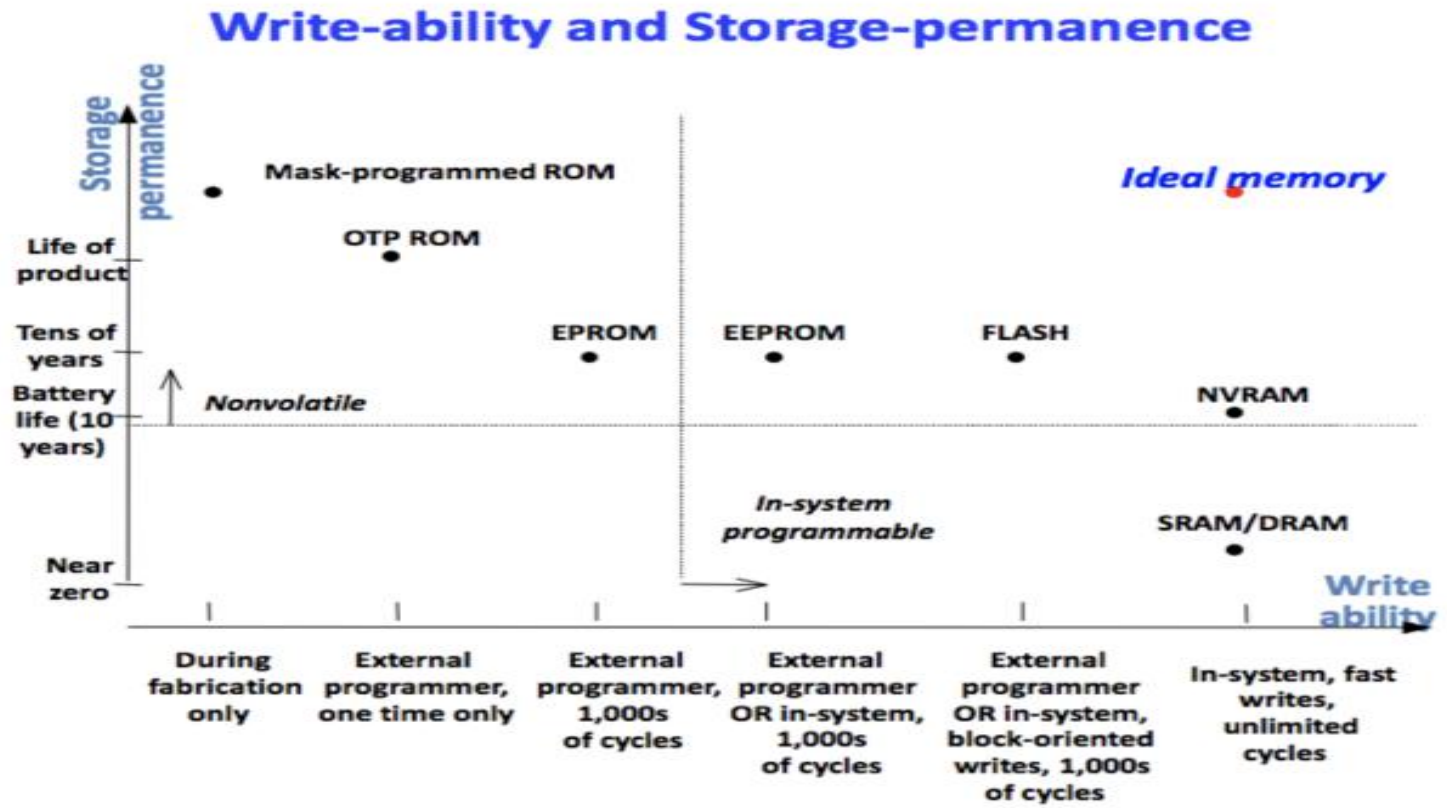
Table 1. Characteristics of the various memory types

Type	Volatile ?	Writeable?	Erase Size	Max Erase Cycles	Cost (per Byte)	Speed
SRAM	Yes	Yes	Byte	Unlimited	Expensive	Fast
DRAM	Yes	Yes	Byte	Unlimited	Moderate	Moderate
Masked ROM	No	No	n/a	n/a	Inexpensive	Fast
PROM	No	Once, with a device programmer	n/a	n/a	Moderate	Fast
EPROM	No	Yes, with a device programmer	Entire Chip	Limited (consult datasheet)	Moderate	Fast
EEPROM	No	Yes	Byte	Limited (consult datasheet)	Expensive	Fast to read, slow to erase/write
Flash	No	Yes	Sector	Limited (consult datasheet)	Moderate	Fast to read, slow to erase/write
NVRAM	No	Yes	Byte	Unlimited	Expensive (SRAM + battery)	Fast

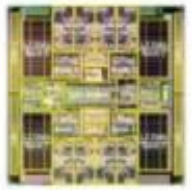
Hybrid Memory

- As memory technology has matured in recent years, the line between RAM and ROM has blurred. Now, several types of memory combine features of both. These devices do not belong to either group and can be collectively referred to as hybrid memory devices. Hybrid memories can be read and written as desired, like RAM, but maintain their contents without electrical power, just like ROM. Two of the hybrid devices, EEPROM and flash, are descendants of ROM devices. These are typically used to store code. The third hybrid, NVRAM, is a modified version of SRAM. NVRAM usually holds persistent data.
- EEPROMs are electrically erasable and programmable. Internally, they are similar to EPROMs, but the erase operation is accomplished electrically, rather than by exposure to ultraviolet light. Any byte within an EEPROM may be erased and rewritten. Once written, the new data will remain in the device forever--or at least until it is electrically erased. The primary tradeoff for this improved functionality is higher cost, though write cycles are also significantly longer than writes to a RAM. So you wouldn't want to use an EEPROM for your main system memory.
- Flash memory combines the best features of the memory devices described thus far. Flash memory devices are high-density, low-cost, nonvolatile, fast (to read, but not to write), and electrically reprogrammable. These advantages are overwhelming, and, as a direct result, the use of flash memory has increased dramatically in embedded systems. From a software viewpoint, flash and EEPROM technologies are very similar. The major difference is that flash devices can only be erased one sector at a time, not byte-by-byte. Typical sector sizes are in the range of 256 bytes to 16KB. Despite this disadvantage, flash is much more popular than EEPROM and is rapidly displacing many of the ROM devices as well.

Storage permanence



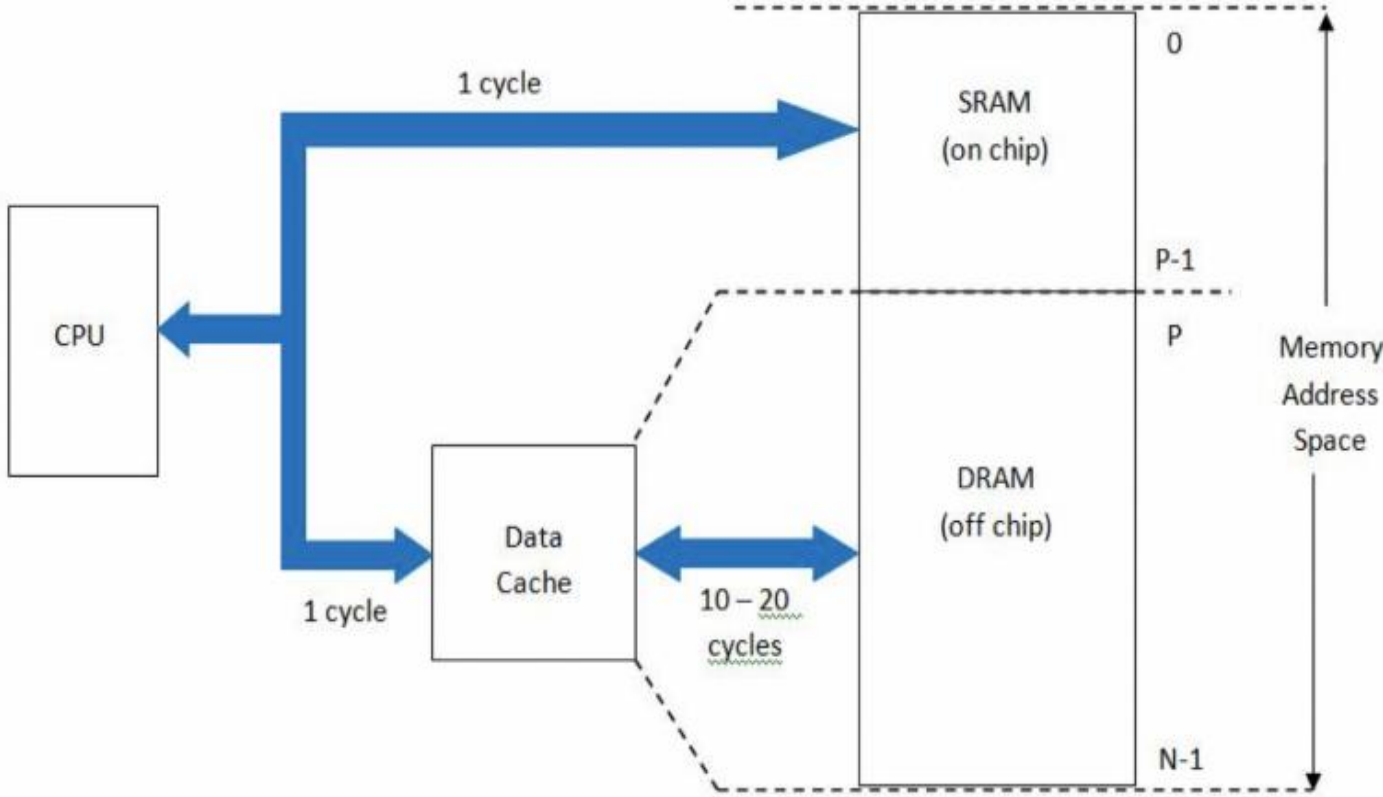
Memory Latency



	On-chip memory (SRAM)	Off-chip memory (DRAM)	Solid State Disk (Flash Memory)	Secondary Storage (HDD)
Latency: (Cycles)	1~30	100~300	25000~2000000	>5000000

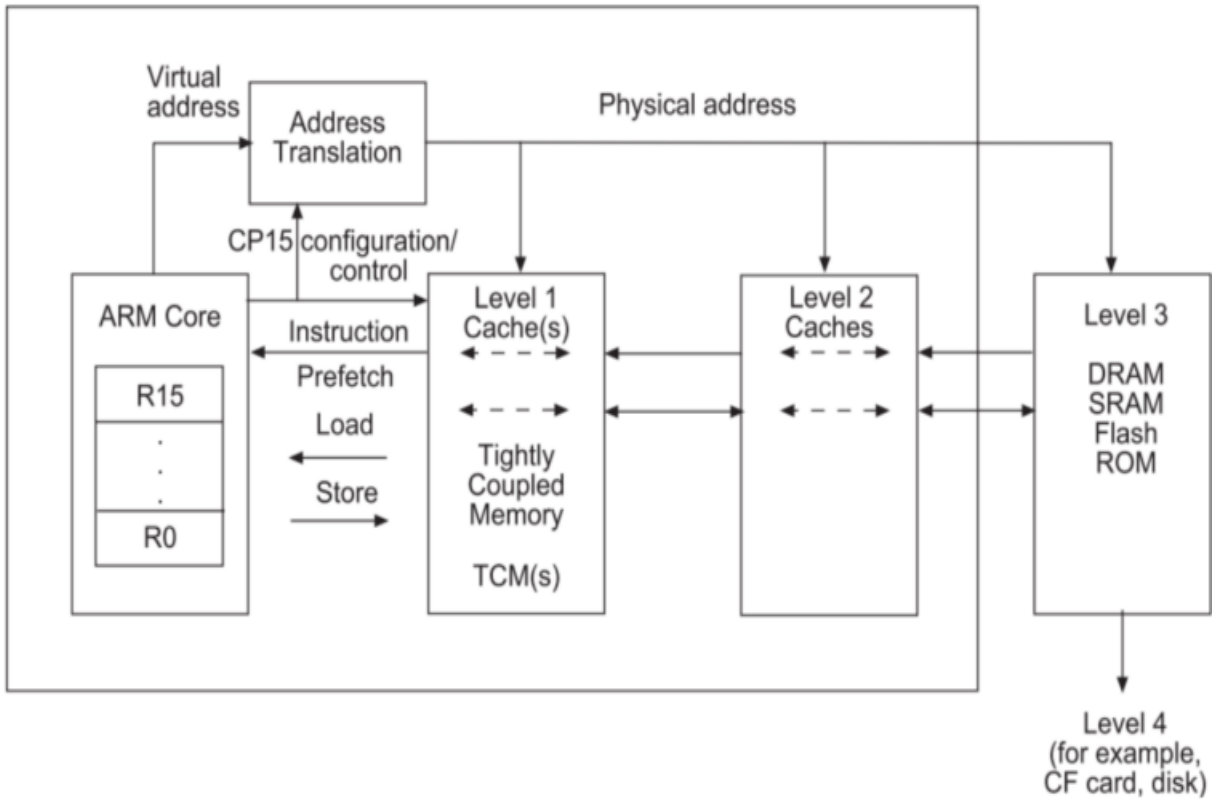
Memory Caches

- Some memories are accessed before others.
- The close memory duplicates data in the distant memory with the hardware automatically handling the copying to and from, then it is called a cache.
- Cache memory is RAM that a microprocessor can access more quickly than it can access regular RAM.
- For embedded applications with tight real-time constraints, cache timing behavior can vary substantially.



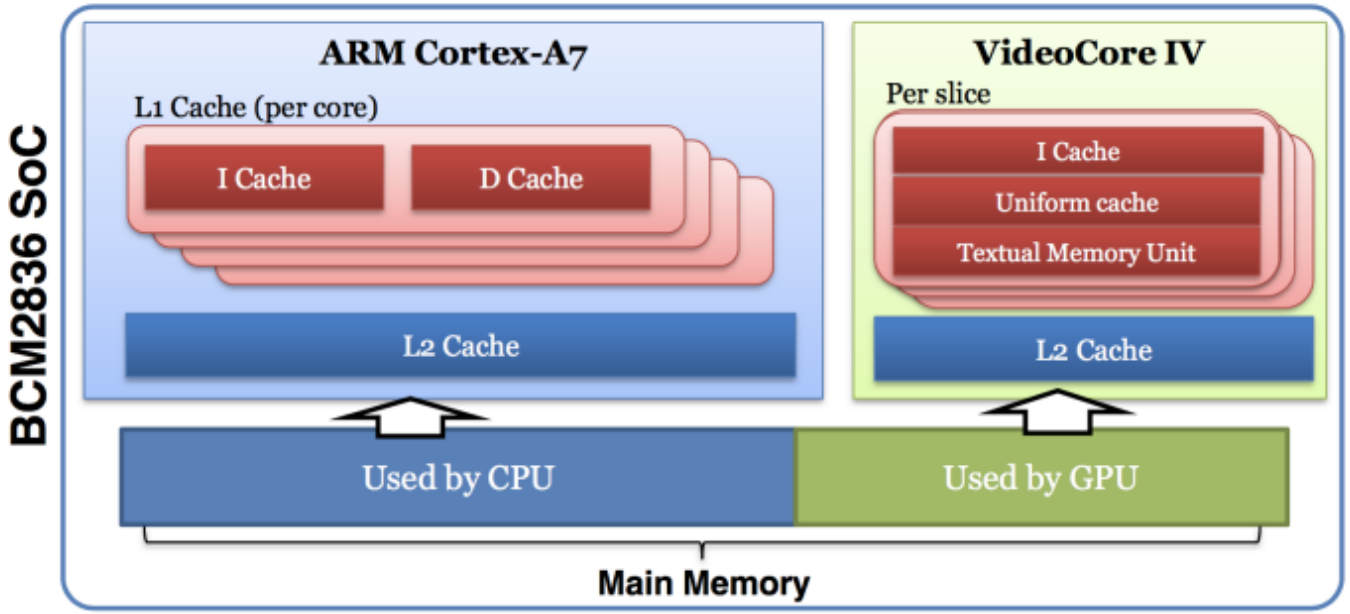
ARM Memory Caches

- Level 1 (L1) cache is extremely fast but relatively small, and is usually embedded in the processor chip (CPU).
- Level 2 (L2) cache is often more capacious than L1; it may be located on the CPU or on a separate chip.
- Level 3 (L3) cache is typically specialized memory that works to improve the performance of L1 and L2. It can be significantly slower than L1 or L2, but is usually double the speed of RAM. In the case of multicore processors, each core may have its own dedicated L1 and L2 cache, but share a common L3 cache



Raspberry Pi2 - Memory Architecture

- Broadcom BCM2836 SoC
- CPU: Quad-core Cortex-A7: L1 and L2 cache
- GPU: VideoCore IV Processor: exclusive memory system
- Main Memory: 1GB RAM : Shared by CPU and GPU



Thank You