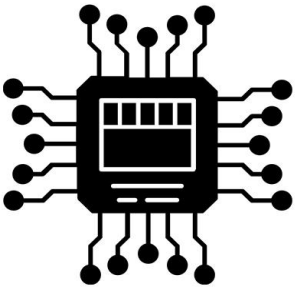

قسم الامن السيبراني

DEPARTMENT OF CYBER SECURITY

SUBJECT:

Microprocessor

CLASS:

SECOND

LECTURER:

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LECTURE: (2)

Microprocessor Architecture

Lecture 2: Microprocessor Architecture

1. Introduction

The Intel 8086 microprocessor represents a major milestone in the evolution of microprocessor technology. It was designed by Intel in 1976 as an enhanced and more powerful successor to the Intel 8085. Unlike the 8085, which is an 8-bit microprocessor, the 8086 is a **16-bit microprocessor**, meaning that its Arithmetic Logic Unit (ALU), internal registers, and data processing capabilities are designed to operate on 16-bit binary words.

The 8086 microprocessor was specifically developed to overcome the limitations of earlier 8-bit processors, particularly in terms of memory addressing capacity, processing speed, and instruction set richness. By introducing a **20-bit address bus**, the 8086 can address up to **1 MB of memory**, which was a significant advancement at the time and laid the foundation for modern x86-based systems.

2. General Features of the 8086 Microprocessor

The most important features of the Intel 8086 microprocessor are summarized below:

1. The 8086 is a **16-bit microprocessor**, where the ALU and internal registers operate on 16-bit data words.
2. It has a **20-bit address bus**, allowing it to access up to ($2^{\wedge 20}$ = 1 MB) of memory locations.
3. It uses a **16-bit data bus**, enabling the processor to read or write 16 bits of data at a time from memory or I/O devices.
4. The processor provides **14 internal 16-bit registers**, which are used for data storage, addressing, and control operations.
5. The operating frequency of the 8086 ranges between **6 MHz and 10 MHz**.
6. It employs a **multiplexed address and data bus**, where lines AD0–AD15 are shared for address and data transmission, and A16–A19 are multiplexed with status signals.
7. The 8086 includes an **instruction queue** capable of storing up to **six bytes of prefetched instructions**, improving execution speed through pipelining.
8. It supports **instruction prefetching**, allowing instruction fetching and execution to overlap.
9. The processor operates with a **+5V power supply**.
10. It supports **two modes of operation**: Minimum Mode (single-processor systems) and Maximum Mode (multiprocessor systems).

3. Comparison Between 8085 and 8086 Microprocessors

Table 2.1: Comparison Between Intel 8085 and Intel 8086

Feature	8085	8086
Processor Size	8-bit	16-bit
Address Bus	16-bit	20-bit
Maximum Memory	64 KB	1 MB
Instruction Queue	Not available	6-byte queue
Pipelining	Not supported	Supported
I/O Addressing	(2^{8} = 256)	(2^{16} = 65,536)
Operation Modes	Single mode	Minimum and Maximum modes
Cost	Lower	Higher

This comparison clearly shows that the 8086 provides significant architectural and performance improvements over the 8085, particularly in memory addressing, instruction execution speed, and system scalability.

4. Internal Architecture of the 8086 Microprocessor

The internal architecture of the 8086 microprocessor is based on the concept of **parallel processing**. Instead of executing tasks sequentially, the processor divides responsibilities among multiple internal units that operate simultaneously. This design approach significantly improves system performance.

The 8086 architecture consists of two major functional units:

1. **Bus Interface Unit (BIU)**
2. **Execution Unit (EU)**

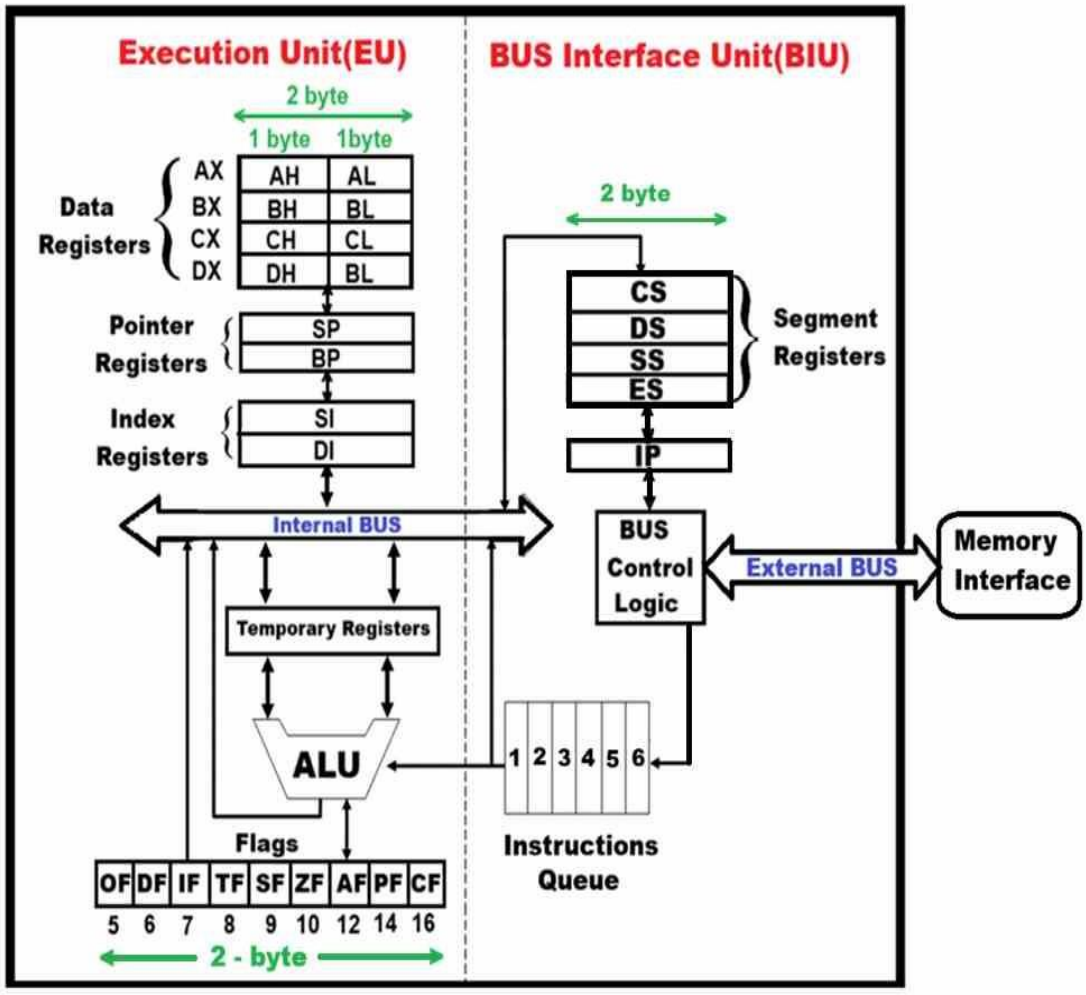

Figure 2.1: Internal Architecture of the 8086 Microprocessor

5. Bus Interface Unit (BIU)

The Bus Interface Unit (BIU) is responsible for all external bus operations. It provides a **16-bit bidirectional data bus** and a **20-bit address bus**, enabling communication with memory and I/O devices.

The primary responsibilities of the BIU include:

1. Fetching instructions from main memory.
2. Supporting instruction queuing using a 6-byte instruction queue.
3. Generating and sending memory and I/O addresses.
4. Reading data from memory or I/O ports.
5. Writing data to memory or I/O ports.

To improve performance, the BIU implements an **instruction stream queue**, which enables pipelined architecture. While the Execution Unit executes the current instruction, the BIU prefetches the next instructions from memory. This overlapping of fetch and execution phases increases overall instruction throughput.

From an examination perspective, the instruction queue and its role in pipelining are considered **core concepts** and are frequently assessed in both theoretical and objective questions.

6. Execution Unit (EU)

The Execution Unit (EU) is responsible for decoding and executing instructions provided by the BIU. It does **not directly communicate with external memory or I/O devices**; instead, it relies on the BIU for all such operations.

The EU consists of the following components:

- **Arithmetic Logic Unit (ALU)**
- **General-purpose registers**
- **Flag register (status and control flags)**
- **Temporary internal registers**

The EU extracts instructions from the instruction queue, decodes them, generates the required operands, and performs the specified operations. During instruction execution, the EU continuously monitors and updates the flag register based on the results of operations.

This separation between BIU and EU is a fundamental design feature of the 8086 and forms the basis for its pipelined execution model.

7. 8086 Pin Configuration

The Intel 8086 was the first 16-bit microprocessor available in a **40-pin Dual Inline Package (DIP)**. Each pin has a specific function related to data transfer, address generation, control signaling, or processor configuration.

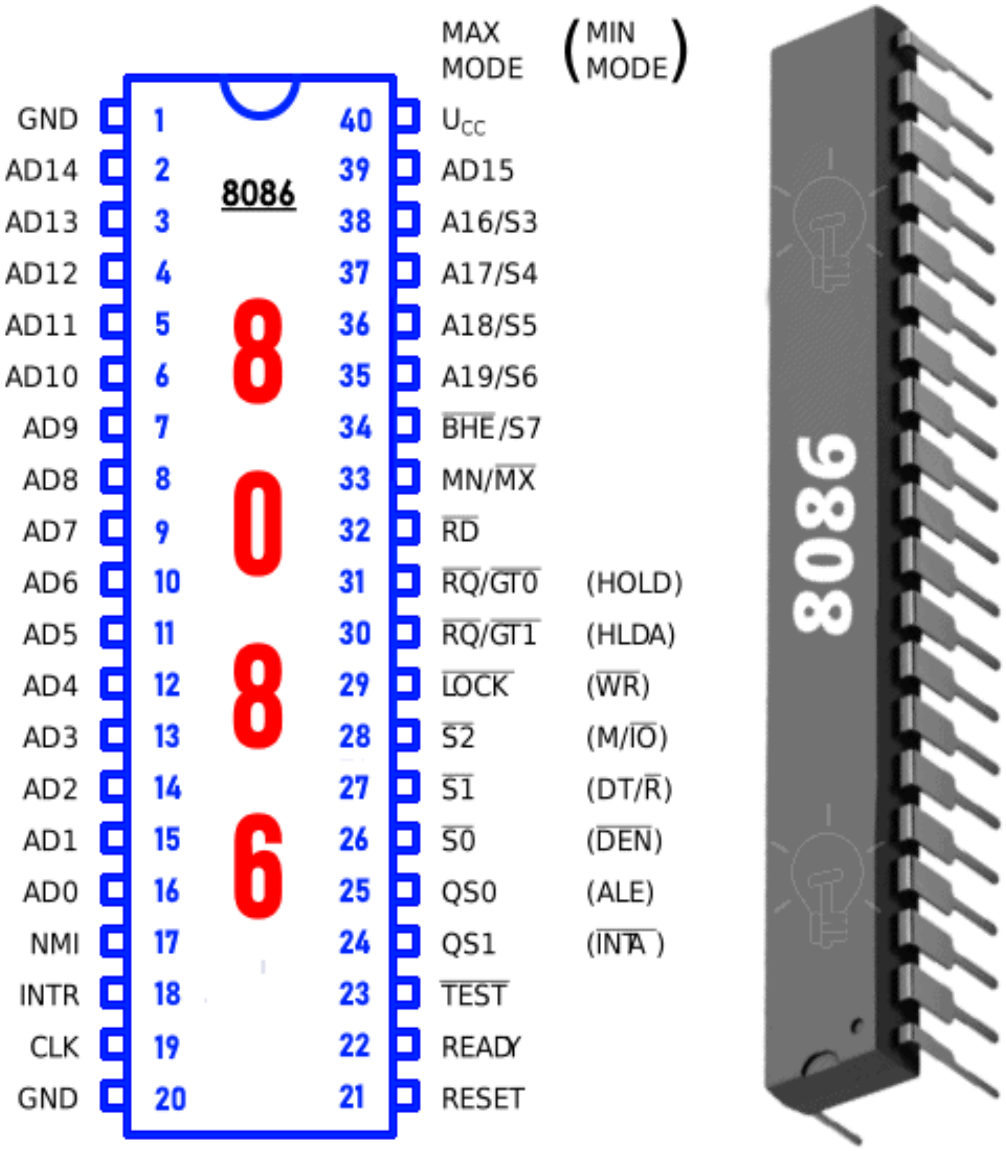

Figure 2.2: Pin Diagram of the 8086 Microprocessor

7.1 Important Pins and Signals

1. **MN/M$\bar{X}$ (Pin 33):** Selects the operating mode. Logic high selects Minimum Mode, while logic low selects Maximum Mode.
2. **AD0–AD15:** Multiplexed address/data bus. Carries address during the first clock cycle and data during subsequent cycles.
3. **A16–A19 / S3–S6:** Address/status bus lines used for higher-order address bits and status signals.
4. **R$\bar{D}$ (Pin 32):** Active-low signal used for memory or I/O read operations.

5. **READY (Pin 22):** Indicates whether an external device is ready for data transfer; low signal introduces wait states.
6. **RESET (Pin 21):** Active-high signal used to restart processor execution.
7. **M/IO̅ (Pin 28):** Distinguishes between memory and I/O operations.
8. **WR̅ (Pin 29):** Active-low signal used for write operations.
9. **QS1 and QS0:** Instruction queue status signals indicating the state of the instruction queue.

Table 2.2: Queue Status Signals

QS1	QS0	Description
0	0	No operation
0	1	First opcode byte
1	0	Queue empty
1	1	Subsequent opcode byte

10. **S0, S1, S2:** Status signals used by the 8288 bus controller to generate control signals in Maximum Mode.

S2	S1	S0	Status
0	0	0	Interrupt acknowledgement
0	0	1	I/O Read
0	1	0	I/O Write
0	1	1	Halt
1	0	0	Opcode fetch
1	0	1	Memory read
1	1	0	Memory write
1	1	1	Passive

11. **LOCK̅:** Prevents other processors from gaining control of the system bus during critical operations.

8. Summary and Examination Notes

- The 8086 is a 16-bit processor with a 20-bit address bus.
- BIU and EU separation enables pipelining and faster execution.
- Instruction queue and segmentation are **high-priority examination topics**.
- Pin functions are frequently tested in objective and short-answer questions.

This lecture establishes the architectural foundation required for understanding addressing modes, instruction sets, and assembly language programming in subsequent lectures.

Check your understanding (MCQ Quastions)

□ Easy questions

Q1. The Intel 8086 microprocessor is classified as a:
A) 8-bit processor
B) 16-bit processor
C) 32-bit processor
D) 64-bit processor
□ **Answer: B**

Q2. The address bus width of the 8086 microprocessor is:
A) 8-bit
B) 16-bit
C) 20-bit
D) 24-bit
□ **Answer: C**

Q3. The maximum memory that can be accessed by the 8086 is:
A) 64 KB
B) 256 KB
C) 512 KB
D) 1 MB
□ **Answer: D**

Q4. The data bus width of the 8086 is:
A) 8-bit
B) 12-bit
C) 16-bit
D) 20-bit
 Answer: C

Q5. The microprocessor 8086 was designed by:
A) Motorola
B) AMD
C) IBM
D) Intel
 Answer: D

Q6. The 8086 supports how many modes of operation?
A) One
B) Two
C) Three
D) Four
 Answer: B

Q7. Minimum mode of 8086 is suitable for:
A) Multiprocessor systems
B) Distributed systems
C) Single processor systems
D) Embedded controllers
 Answer: C

Q8. Maximum mode of 8086 is mainly used in:
A) Single CPU systems
B) Multiprocessor systems
C) Low-cost systems
D) Microcontrollers
 Answer: B

Q9. The instruction queue size in 8086 is:
A) 2 bytes
B) 4 bytes
C) 6 bytes
D) 8 bytes
 Answer: C

Q10. Which unit fetches instructions from memory in 8086?
A) ALU

B) EU
C) BIU
D) Control Unit
 Answer: C

Q11. The execution of instructions is performed by:
A) BIU
B) EU
C) Memory
D) Control Bus
 Answer: B

Q12. Which of the following improves execution speed in 8086?
A) Large registers
B) Instruction queue
C) High voltage supply
D) Serial processing
 Answer: B

Q13. The supply voltage required for 8086 is:
A) +3.3V
B) +12V
C) −5V
D) +5V
 Answer: D

Q14. The 8086 uses which type of packaging?
A) PGA
B) QFP
C) DIP (40-pin)
D) BGA
 Answer: C

Q15. The architecture of 8086 is based on:
A) Serial processing
B) Parallel processing
C) Optical processing
D) Distributed processing
 Answer: B

Moderate questions

Q16. Which unit contains the instruction queue?
A) EU
B) ALU
C) BIU
D) Control Unit
 Answer: C

Q17. The main function of the EU is to:
A) Fetch instructions
B) Decode and execute instructions
C) Generate addresses
D) Control I/O devices
 Answer: B

Q18. Which registers are part of the Execution Unit?
A) Segment registers
B) General-purpose registers
C) Temporary registers
D) All of the above
 Answer: D

Q19. Instruction pipelining in 8086 is achieved by:
A) ALU
B) Control Unit
C) Instruction Queue
D) Segment Registers
 Answer: C

Q20. The BIU communicates with memory using:
A) Internal bus only
B) External bus
C) ALU
D) Stack
 Answer: B

Q21. AD0–AD15 pins are used for:
A) Address only
B) Data only
C) Address and Data
D) Control signals
 Answer: C

Q22. During the first clock cycle, AD0–AD15 carry:
A) Data

B) Address
C) Opcode
D) Status
 Answer: B

Q23. A16–A19 pins later act as:
A) Data lines
B) Control lines
C) Status lines
D) Clock lines
 Answer: C

Q24. RD signal is used to indicate:
A) Write operation
B) Reset operation
C) Read operation
D) Interrupt
 Answer: C

Q25. READY signal is used to:
A) Reset CPU
B) Insert wait states
C) Enable ALU
D) Disable interrupts
 Answer: B

Q26. M/IO signal distinguishes between:
A) Read and write
B) Instruction and data
C) Memory and I/O operations
D) Internal and external bus
 Answer: C

Q27. WR signal is active during:
A) Memory read
B) I/O read
C) Write operation
D) Opcode fetch
 Answer: C

Q28. QS0 and QS1 signals indicate:
A) Interrupt status
B) Queue status
C) Memory status

D) Power status
 Answer: B

Q29. LOCK signal is used to:
A) Reset CPU
B) Stop clock
C) Prevent bus access by other processors
D) Enable interrupts
 Answer: C

Q30. The 8086 instruction queue helps in:
A) Reducing memory size
B) Increasing power consumption
C) Speeding up execution
D) Increasing voltage
 Answer: C

Difficult questions

Q31. Which combination correctly represents memory addressing capability of 8086?
A) 2^{16} = 64 KB
B) 2^{18} = 256 KB
C) 2^{20} = 1 MB
D) 2^{24} = 16 MB
 Answer: C

Q32. Pipelining in 8086 mainly overlaps:
A) Decode and Execute
B) Fetch and Execute
C) Fetch and Decode
D) Read and Write
 Answer: B

Q33. Which unit generates physical addresses in 8086?
A) EU
B) ALU
C) BIU
D) Stack Pointer
 Answer: C

Q34. If instruction queue is empty, the BIU will:
A) Halt execution
B) Stop fetching instructions
C) Fetch new instructions
D) Reset processor
 Answer: C

Q35. Which signal combination indicates "Opcode Fetch"?
A) S2=0, S1=0, S0=0
B) S2=1, S1=0, S0=0
C) S2=0, S1=1, S0=1
D) S2=1, S1=1, S0=1
 Answer: B

Q36. Compared to 8085, 8086 introduces:
A) Lower speed
B) Instruction queue
C) Fewer registers
D) Smaller memory
 Answer: B

Q37. The EU requests BIU to perform memory access using:
A) Flags
B) Clock
C) Control signals
D) Registers only
 Answer: C

Q38. Multiplexing address and data buses helps in:
A) Increasing memory
B) Reducing pin count
C) Increasing voltage
D) Simplifying ALU
 Answer: B

Q39. Which is NOT a responsibility of BIU?
A) Instruction fetch
B) Instruction decode
C) Data transfer
D) Address generation
 Answer: B

Q40. The main architectural advantage of splitting 8086 into BIU and EU is:
A) Reduced cost

B) Increased power
C) Parallel execution
D) Smaller size
 Answer: C