MODULE DESCRIPTION FORM

نموذج وصف المادة الدراسية

Module Information معلومات المادة الدراسية					
Module Title	**Digital Logic Design**			**Module Delivery**	
Module Type	**Core**				
Module Code	**UOMU0208021**			✓ **Theory** **Lecture** ✓ **Lab** ✓ **Tutorial** **Practical** **Seminar**	
ECTS Credits	**6**				
SWL (hr/sem)	**150**				
Module Level	1		**Semester of Delivery**	2	
Administering Department	CSET		**College**	TECAI	
Module Leader	Rami qays malk		**e-mail**	Rami.qays@uomus.edu.iq	
Module Leader's Acad. Title			**Module Leader's Qualification**		
Module Tutor	Name (if available)		**e-mail**		
Peer Reviewer Name			**e-mail**		
Scientific Committee Approval Date			**Version Number**	1.0	

Relation with other Modules العلاقة مع المواد الدراسية الأخر ى			
Prerequisite module	None	**Semester**	
Co-requisites module	None	**Semester**	

Module Aims, Learning Outcomes and Indicative Contents أهداف المادة الدراسية ونتائج التعلم والمحتويا ت الإرشادي ة	
Module Aims أهداف المادة الدراسي ة	1. 2. To be able to deal with the number systems and codes. 3. 4. To understand the functionality of logic gates. 5. To have the skill to use the logic gates in designing logic circuits. To have the skill to simplify the digital circuits. To learn the simplification process, Boolean expression, Demorgans law, and Karnaugh map. 6. To understand the principles for designing logic circuits. 7. To understand adder, subtractor, decoder, encoder, multiplexer, demultiplexer, and comparator circuits.
Module Learning Outcomes مخرجات التعلم للمادة الدراسي ة	Recognize each type of number system. Identify the process of converting between number systems. 1. 2. Summarize the types of logic gates. 3. 4. Discuss the use of each gate. 5. 6. Describe the design of a logic circuit by using logic gates. 7. 8. Explain the simplification processes. 9. Explain Boolean expression and Demorgan's law. 10. Explain the Karnaugh map for different numbers of bits. 11. Discuss the design of the logic circuit before and after simplification. Explain the combinational logic circuit. 12. Identify the adder, subtractor, decoder, encoder, multiplexer, demultiplexer. 13. Identify the basic circuit elements and their applications. Identify the basic concepts of flip flops and its applications in synchronous and asynchronous counters

Indicative Contents المحتويات الإرشادية	Indicative content includes the following. Number systems - decimal, binary, octal, hexadecimal number system, conversion, operation. [10 hrs] Codes- excess-3, gray code, conversions, operations, complements [5 hrs] Logic gates-NOT, AND, OR, NOR, NAND, XOR, XNOR. [5 hrs] Logic simplification- Boolean theorem and Demorgans law. [10 hrs] Karnaugh map-SOP, POS, and don't care. [15 hrs]
	Arithmetic operations Part A- adder, parallel binary adder, subtractor, addersubtractor. [10 hrs] Arithmetic operations Part B- multiplexer, demultiplexer, decoder, encoder. [10 hrs] Flip Flops types and applications [4] Synchronous and Asynchronous Counters [6]

Learning and Teaching Strategies استراتيجيات التعلم والتعلي م	
Strategies	Type something like: The main strategy that will be adopted in delivering this module is to encourage students' participation in the exercises while at the same time refining and expanding their critical thinking skills. This will be achieved through classes, interactive tutorials, and by considering the type of simple experiments involving some interesting sampling activities for the students.

Student Workload (SWL) الحمل الدراسي للطالب			
Structured SWL (h/sem) الحمل الدراس ي المنتظم للطالب خلال الفص ل	79	**Structured SWL (h/w)** الحمل الدراسي المنتظم للطالب أسبوعيا	5
Unstructured SWL (h/sem) الحمل الدراس ي غير المنتظم للطالب خلال الفص ل	71	**Unstructured SWL (h/w)** الحمل الدراسي غير المنتظم للطالب أسبوعيا	5
Total SWL (h/sem) الحمل الدراس ي الكل ي للطال ب خلال الفص ل	150		

Module تقييمEvaluation المادة الدراسي ة					
		Time/Number	**Weight (Marks)**	**Week Due**	**Relevant Learning Outcome**
Formative assessment	**Quizzes**	2	10% (10)	5, 10	LO #1, 2, 10 and 11
	Assignments	2	10% (10)	2, 12	LO # 3, 4, 6 and 7
	Projects / Lab.	7	15% (15)	Continuous	
	Report	1	5% (5)	13	LO # 5, 8 and 10
Summative assessment	**Midterm Exam**	2hr	10% (10)	7	LO # 1-7
	Final Exam	4hr	50% (40+10)	16	All
Total assessment			100% (100 Marks)		

Delivery Plan (Weekly Syllabus) المنهاج الاسبوعي النظر ي	
	Material Covered
Week 1	Number systems (decimal, binary, octal, conversions, operations)
Week 2	Number systems (hexadecimal, BCD, conversions, operations)
Week 3	Number systems (excess-3, gray code, conversions, operations, complements)
Week 4	Logic gates (AND, OR, NOT, NAND, NOR, XOR, XNOR)
Week 5	Logic simplification (Boolean theorem)
Week 6	Logic simplification (Demorgan's theorem)
Week 7	Karnaugh maps (2-variables, 3-variables)
Week 8	Karnaugh maps (4-variables (SOP, POS, don't care))
Week 9	Karnaugh maps (5-variables, (SOP, POS, don't care))
Week 10	Arithmetic operations (adder, parallel binary adder)
Week 11	Arithmetic operations (subtractor, adder-subtractor circuit)
Week 12	Arithmetic operations (decoder, encoder)
Week 13	Arithmetic operations (Multiplexer, Demultiplexer)
Week 14	Flip-flop types and operation

Week 15	Synchronous and Asynchronous Counter
Week 16	**Preparatory week before the Final Exam**

Delivery Plan (Weekly Lab. Syllabus)

المنهاج الاسبوعي للمختب ر

	Material Covered
Week 1	Lab 1: logic gates (NOT, AND, OR)
Week 2	Lab 2: Logic gates (NOR.NAND)
Week 3	Lab 3: Logic gates (XOR, XNOR)
Week 4	Lab 4: Boolean theorem
Week 5	Lab 5: Demorgan's law
Week 6	Lab 6: Karnaugh map
Week 7	Lab 7: SOP
Week 8	Lab 8: POS, don't care
Week 9	Combinational circuit (half adder, full adder)
Week 10	Combinational circuit (Half subtractor, full subtractor)
Week 11	Decoder and Encoder circuits
Week 12	Multiplexer and Demultiplexer circuits
Week 13	Flip Flop Latch
Week 14	Counters

Learning and Teaching Resources

مصادر التعلم والتدري س

	Text	**Available in the Library?**
Required Texts	Digital Fundamentals by Floyed	Yes
Recommended Texts	Digital circuit analysis and design with Simulink modeling by Steven T. Karris	No
Websites	https://www.coursera.org/browse/physical-science-and-engineering/computerengineering	

Grading Scheme مخطط الدرجا ت				
Group	**Grade**	التقدير	**Marks (%)**	**Definition**
Success Group (50 - 100)	**A -** Excellent	امتياز	90 - 100	Outstanding Performance
	B - Very Good	جيد جدا	80 - 89	Above average with some errors
	C - Good	جيد	70 - 79	Sound work with notable errors
	D - Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	E - Sufficient	مقبول	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	**FX –** Fail	راسب)قيد المعالجة(	(45-49)	More work required but credit awarded
	F – Fail	راس ب	(0-44)	Considerable amount of work required

Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.