Ministry of Higher Education and Scientific Research - Iraq
Al-Furat Al-Awsat Technical University
Technical College /Al-Mussaib
Department of Electrical Engineering Techniques

MODULE DESCRIPTOR FORM

نموذج وصف المادة الدراسية

Module Information معلومات المادة الدراسية					
Module Title	**DIGITAL TECHNOLOGIES**			**Module Delivery**	
Module Type	**Core**			✓ **Theory** **Lecture** ✓ **Lab** **Tutorial** **Practical** ✓ **Seminar**	
Module Code	**ATU٢٣٠١٢**				
ECTS Credits	٦				
SWL (hr/sem)	١٥٠				
Module Level	١		**Semester of Delivery**	١	
Administering Department	**Department of Electrical Engineering Techniques**		**College**	**Al-Furat Al-Awsat Technical University Technical College /Al-Mussaib**	
Module Leader	Zahraa Emad		**e-mail**	Zahraa.emad@atu.edu.iq	
Module Leader's Acad. Title	Assist. Lect.		**Module Leader's Qualification**	M.Sc.	
Module Tutor	None		**e-mail**	None	
Peer Reviewer Name	None		**e-mail**	None	
Scientific Committee Approval Date	٠١/٠٦/٢٠٢٣		**Version Number**	١,٠	

Relation with other Modules العلاقة مع المواد الدراسية الأخرى			
Prerequisite module	None	**Semester**	
Co-requisites module	None	**Semester**	

Module Aims, Learning Outcomes and Indicative Contents أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية	
Module Objectives أهداف المادة الدراسية	**١-Training students on the basics of logical circuits used in electronic computers and how they work.** **٢- Building logical circuits and learning about computer operation.**
Module Learning Outcomes مخرجات التعلم للمادة الدراسية	١. Learning about the different number systems. ٢. Learning the arithmetic operations related to different number systems. ٣. Learning the different logic gates of computer system and their work. ٤. Ability to design, simplify and implement different logical and arithmetic circuits that considered the basic of digital system. ٥. Ability to design, simplify and implement different sequential circuits, counters and shift registers.
Indicative Contents المحتويات الإرشادية	Indicative content includes the following: • Part ١ – Numbers Systems, Operations, and Codes Different Number Systems, Data representation (integer and fraction) using different number systems. Conversion Between Different Numbers Systems. Arithmetic operations using different number systems, and Digital Codes (BCD, Parity, Gray, etc.) [١٠ hrs] • Part ٢- Logic Gates The Inverter (NOT Gate), AND Gate, OR Gate, NAND Gate, NOR Gate, the Exclusive-OR Gate and Exclusive-NOR Gates. [٨ hrs] • Part ٣ Boolean Algebra and Logic Simplification Boolean Operations and Expressions, Laws and Rules of Boolean Algebra, Simplification Using Boolean Algebra, DeMorgan's theorems,The Karnaugh Map (١, ٢ , ٣ and ٤ variables) , SOP and POS Minimization. [٨ hrs] • Part ٤ Combinational Logic Analysis Basic Combinational Logic Circuits, Implementing Combinational Logic, Combinational Logic Using NAND and NOR Gates, Logic Circuit Operation with Pulse Waveform Inputs. [١٠ hrs] Revision problem classes [١٠ hrs] • Part ٥ – Functions of Combinational Logic. Half , Full and Parallel Binary Adders and Subtractors. ١'s and ٢'s Complement Subtractor, ٢'s Complement Adder-Subtractor, BCD Adder, etc. Comparators, Decoders, Encoders, Multiplexers, Demultiplexer [١٠ hrs] • Part ٦- Latches, Flip-Flops, and Timers. Latches, Edge-Triggered Flip-Flops. Flip-Flop operating (R-S, T, J-K ,D) [١٢ hrs] • Part ٧Counters Synchronous Counters, Asynchronous Counters. Design of Counters. [٨ hrs] • Part ٨ Shift Registers Basic Shift Register Operations: SISO, SIPO, PISO, PIPO, Bidirectional and special Types Shift Register. [٦ hrs] • Revision problem classes [٦ hrs] • Part ٩– Microprocessor Introduction to Microprocessor: component of microprocessor, Microprocessor architecture [٦ hrs]

Learning and Teaching Strategies استراتيجيات التعلم والتعليم	
Strategies	The main strategy that will be adopted in delivering this module is to encourage students' participation in the exercises, while at the same time refining and expanding their critical thinking skills. This will be achieved through classes, interactive tutorials and by considering types of simple experiments involving some sampling activities that are interesting to the students.

Student Workload (SWL) الحمل الدراسي للطالب محسوب لـ ١٥ اسبوعا			
Structured SWL (h/sem) الحمل الدراسي المنتظم للطالب خلال الفصل	٩٣	**Structured SWL (h/w)** الحمل الدراسي المنتظم للطالب أسبوعيا	٦,٢
Unstructured SWL (h/sem) الحمل الدراسي غير المنتظم للطالب خلال الفصل	٥٧	**Unstructured SWL (h/w)** الحمل الدراسي غير المنتظم للطالب أسبوعيا	٣,٨
Total SWL (h/sem) الحمل الدراسي الكلي للطالب خلال الفصل	١٥٠		

Module Evaluation تقييم المادة الدراسية					
		Time/Number	**Weight (Marks)**	**Week Due**	**Relevant Learning Outcome**
Formative assessment	**Quizzes**	٤	١٠٪ (١٠)	٣,٥ and ١٠	١,٣,and ٤
	Assignments	٧	١٠٪ (١٠)	٢ and ١٢	٢,٣
	Projects / Lab.	٩	١٠٪ (١٠)	Continuous	All
	Report	٨	١٠٪ (١٠)	٢ and ١٢	LO #٣, #٤ and #٥
Summative assessment	**Midterm Exam**	٢hr	١٠٪ (١٠)	٨	LO #١ - #٥
	Final Exam	٣hr	٥٠٪ (٥٠)	١٥	All
Total assessment			١٠٠٪ (١٠٠ Marks)		

Delivery Plan (Weekly Syllabus) المنهاج الاسبوعي النظري

	Material Covered
Week ١	Introduction - Difference between Circuit Theory and Field Theory
Week ١	• General number formula: Binary, octal, decimal and hexadecimal numbers
Week ٢	• Arithmetic operations in different number system
Week ٣	• complements, binary codes, BCD, Ex-٣, Gray codes
Week ٤	• Basic definitions, basic theorem and properties, Boolean functions
Week ٥	• Canonical and Standard forms Digital Logic Gates
Week ٦	• Karanough Maps: AND- OR implementation, don't care conditions
Week ٧	• Subtractions, half and full adders and subtractions, binary parallel address
Week ٨	• decoders, encoders, comparators
Week ٩,١٠	• multiplexers and demultiplexers
Week ١١	• Flip-flops (RS, T, D, JK …) • Master slave FF, counter • shift registers
Week ١٢,١٣	• Introduction to Microprocessor • Microprocessor architecture
Week ١٤	• component of microprocessor
Week ١٥	• Final Examination

Delivery Plan (Weekly Lab. Syllabus)

المنهاج الاسبوعي للمختبر

	Material Covered
Week ١	• Lab ١: Introduction to digital laboratory kit operation • Lab ٢: Logic Gates (AND, OR, NOT, NAND, NOR).
Week ٢	• Lab ٣: Logic Gates (XOR, XNOR). • Lab ٤: De Morgan's Theorems 1st and 2nd Laws.
Week ٣	• Lab ٥: Designing a combinational Logic circuit. • Lab ٦: The realization of the Boolean equation.
Week ٤	• Lab ٩: Half Binary Subtractor. • Lab ١٠: Full Binary Subtractor.
Week ٥	• Lab ١١:Binary comparator
Week ٦	• Lab ١٢: ٢'s Complement Adder- Subtractor
Week ٧	• Lab ١٣: Flip-Flop.

Learning and Teaching Resources

مصادر التعلم والتدريس

	Text	Available in the Library?
Required Texts	Thomas L. Floyd, Digital Fundamentals, 11th Edition, Pearson Education 2015	Yes
Recommended Texts	1- Introduction to Digital Logic with Laboratory Exercises/James Feher, 2009.	No

	2- M. Morris Mano, Michael D. Ciletti, Digital Design, 5th edition, Pearson Education 2013.	
Websites	Digital Systems: From Logic Gates to Processors: https://www.coursera.org/learn/digital-systems	

Grading Scheme مخطط الدرجات				
Group	**Grade**	التقدير	**Marks %**	**Definition**
Success Group (٥٠ - ١٠٠)	**A** - Excellent	امتياز	٩٠ - ١٠٠	Outstanding Performance
	B - Very Good	جيد جدا	٨٠ - ٨٩	Above average with some errors
	C - Good	جيد	٧٠ - ٧٩	Sound work with notable errors
	D - Satisfactory	متوسط	٦٠ - ٦٩	Fair but with major shortcomings
	E - Sufficient	مقبول	٥٠ - ٥٩	Work meets minimum criteria
Fail Group (٠ – ٤٩)	**FX** – Fail	راسب (قيد المعالجة)	(٤٥-٤٩)	More work required but credit awarded
	F – Fail	راسب	(٠-٤٤)	Considerable amount of work required

Note: Marks Decimal places above or below ٠,٥ will be rounded to the higher or lower full mark (for example a mark of ٥٤,٥ will be rounded to ٥٥, whereas a mark of ٥٤,٤ will be rounded to ٥٤. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.