

Logic Design - FORM

مفونج ووصف المادة الدراسية

Module Information			
لومات المادة الدراسية			
Module Title	Logic Design		Module Delivery
Module Type	Basic		<input checked="" type="checkbox"/> Theory <input checked="" type="checkbox"/> Lecture <input checked="" type="checkbox"/> Lab <input type="checkbox"/> Tutorial <input type="checkbox"/> Practical <input type="checkbox"/> Seminar
Module Code	UOMU0302024		
ECTS Credits	5		
SWL (hr/sem)	125		
Module Level	1	Semester of Delivery	
Administering Department	الأنظمة الطبية الذكية	College	العلوم
Module Leader	م.م. علي سليم حليم	e-mail	ali.saleem.haleem@uomus.edu.iq
Module Leader's Acad. Title	Assistant lecturer	Module Leader's Qualification	M.Sc.
Module Tutor	م.م. علي سليم حليم	e-mail	ali.saleem.haleem@uomus.edu.iq
Peer Reviewer Name	اد. مهدي عبادي مانع	e-mail	mahdi.ebadi@uomus.edu.iq
Scientific Committee Approval Date	01/06/2023	Version Number	1.0

Relation with other Modules			
للعلاقة مع لومات دراسية الأخرى			
Prerequisite module	None	Semester	
Co-requisites module	None	Semester	

Module Aims, Learning Outcomes and Indicative Contents

هأأاف المأفة الءراسفة وناائج الءعلم والمءءوافاء الإرشاءفة

<p>Module Aims هأفف المأفة الءراسفة</p>	<ul style="list-style-type: none"> - Understanding of the basic principles of logic circuit design - Analyze the behavior of logic digital circuits - Understanding Concepts of Number Systems and Boolean Algebra - Understanding Karnaugh Maps (K-maps) Concepts - Understanding Combinational and Sequential Circuit - Understanding Half and full Subtractor - Understanding Encoder and decoder - Understanding Multiplexers and De-multiplexers - Understanding Decoder Expansion - Understanding Latches - Understanding the Counter
<p>Module Learning Outcomes بؤاء الءعلم للمأفة الءراسفة</p>	<ul style="list-style-type: none"> - Students become familiar with basic digital hardware by constructing simple combinational circuits, and learning troubleshooting skills. - Students should become familiar with logic gates that perform the basic Boolean functions, such as AND, OR, NAND, NOR, Inversion, Exclusive-OR, Exclusive-NOR - Students should become familiar with (K-Maps, Combinational and Sequential Circuit, Half and full Subtractor, Logic Circuits for Full Subtractor, Encoder and decoder, Multiplexers and De-multiplexers, Decoder Expansion, Latches, Counter)
<p>Indicative Contents لامءءوافاء الإرشاءفة</p>	<p>Indicative content includes the following.</p> <ul style="list-style-type: none"> - Introduction and Digital concepts number systems: Decimal, Binary, Octal and Hexadecimal numbers. - Logic gates: (inverter, AND, OR, NANAD, NOR, Exclusive OR and Exclusive NOR) - De Margan's theorems (Laws and theorem of Boolean algebra) - Simplifying logic circuits (sum of products and product of sum) - Simplifying logic circuits: Karnaugh ma - Combinational and Sequential Circuit - Half and full Subtractor - Logic Circuits for Full Subtractor - Encoder and decoder - Multiplexers and De-multiplexers - Decoder Expansion - Latches - the Counter

Learning and Teaching Strategies

ساتراتيجيات التعلم والتعليم

Strategies	Type something like: The main strategy that will be adopted in delivering this module is to encourage students' participation in the exercises, while at the same time refining and expanding their critical thinking skills. This will be achieved through classes, interactive tutorials and by considering type of simple experiments involving some sampling activities that are interesting to the students.
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Student Workload (SWL)

لاحمل لادراسي للطالب

Structured SWL (h/sem) لحمل لادراسي لمنتظم للطالب خلال لافصل	64	Structured SWL (h/w) لحمل لادراسي لمنتظم للطالب أسبوعيا	4
Unstructured SWL (h/sem) لاحمل لادراسي غير لمنتظم للطالب خلال لافصل	61	Unstructured SWL (h/w) لاحمل لادراسي غير لمنتظم للطالب أسبوعيا	4
Total SWL (h/sem) لاحمل لادراسي لأكلي للطالب خلال لافصل	125		

Module Evaluation

قتييم المادة الدراسية

		Time/Number	Weight (Marks)	Week Due	Relevant Learning Outcome
Formative assessment	Quizzes	2	10% (10)	5, 10	LO #1, 2, 10 and 11
	Assignments	2	10% (10)	2, 12	LO # 3, 4, 6 and 7
	Projects / Lab.	1	10% (10)	Continuous	
	Report	1	10% (10)	13	LO # 5, 8 and 10
Summative assessment	Midterm Exam	2 hr	10% (10)	7	LO # 1-7
	Final Exam	2hr	50% (50)	16	All
Total assessment			100% (100 Marks)		

Delivery Plan (Weekly Syllabus)

للمناهج الاسبوعي للانظري

	Material Covered
Week 1	<ul style="list-style-type: none"> - Digital and analog quantities. - Binary digits, Logic levels, and digital waveforms. - Basic logic operations - Decimal numbers - Binary numbers - Decimal to binary conversion
Week 2	Number systems <ul style="list-style-type: none"> - Octal numbers. - Hexadecimal numbers. - 1's and 2's complements of binary numbers Binary codes <ul style="list-style-type: none"> - Weighted Codes - Non-Weighted Codes - Binary Coded Decimal Code. - Alphanumeric codes
Week 3	Logic gates <ul style="list-style-type: none"> - The inverter - The AND gate - The OR gate - The NAND gate - The NOR gate - The Exclusive OR - Exclusive NOR
Week 4	Basic principles K-Maps and terminology <ul style="list-style-type: none"> - K-map Simplification for Two Variables - K-map Simplification for Three Variables - K-map Simplification for Four Variables - Karnaugh Maps - Rules of Simplification
Week 5	Combinational and Sequential Circuit <ul style="list-style-type: none"> - Half and full Adder - Difference between Half adder and full adder
Week 6	<ul style="list-style-type: none"> - First test
Week 7	Logic Circuits for Full and Parallel Subtractor
Week 8	Encoder and decoder concept
Week 9	<ul style="list-style-type: none"> - Multiplexers and De-multiplexers
Week 10	Decoder Expansion <ul style="list-style-type: none"> - MUX Expansion

	- DE-MUX Expansion
Week 11	Latches and type of Latches
Week 12	Counter concept and example
Week 13	Apply Counter
Week 14	Second test
Week 15	Project
Week 16	Preparatory week before the final Exam

Delivery Plan (Weekly Lab. Syllabus)

لامنهاج الاسبوع للمختبر

	Material Covered
Week 1	How to Use NI multisim 14.0 program
Week 2	Training to draw Gates and Draw a circuit multi-gate
Week 3	Completion Training to draw Gates and Draw a circuit multi-gate
Week 4-5	Draw K-Maps by using NI multisim program in Logic Lab
Week 6	Completion Draw K-Maps by using NI multisim program in Logic Lab
Week 7	Draw Combinational and Sequential Circuit
Week8	Draw Encoder and decoder
Week9	Exam
Week 10-11	Draw Multiplexers and De-multiplexers
Week 12	Completion Draw Multiplexers and De-multiplexers
Week 13	Assailment (Draw a circuit by using a Multisim)
Week 14	Completion Assailment (Draw a circuit by using a Multisim)
Week 15	Review
Week 16	Exam

Learning and Teaching Resources

ادر التعلم والتدريس

	Text	Available in the Library?
Required Texts	"DIGITAL FUNDAMENTALS"; Thomas L. Floyd; Pearson Prentice Hall™	Yes
Recommended Texts	"DIGITAL FUNDAMENTALS"; Thomas L. Floyd; Pearson Prentice Hall™	Yes
Websites		

Grading Scheme

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Group	Grade	لاتقدير	Marks (%)	Definition
Success Group (50 - 100)	A - Excellent	ماتياز	90 - 100	Outstanding Performance
	B - Very Good	د جدا	80 - 89	Above average with some errors
	C - Good	د	70 - 79	Sound work with notable errors
	D - Satisfactory	تموسط	60 - 69	Fair but with major shortcomings
	E - Sufficient	بول	50 - 59	Work meets minimum criteria
Fail Group (0 - 49)	FX – Fail	لب (قيد المعالجة)	(45-49)	More work required but credit awarded
	F – Fail	لب	(0-44)	Considerable amount of work required

Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.