Ministry of Higher Education and
Scientific Research - Iraq
Al-Mustaqbal University
College of Engineering Technique
Department of Electrical Engineering Technique

MODULE DESCRIPTOR FORM
نموذج وصف المادة الدراسية

Module Information		
معلومات المادة الدراسية		
Module Title	**DIGITAL TECHNOLOGIES**	**Module Delivery**
Module Type	Core	✓ Theory Lecture
Module Code	UOMU0205012	✓ Lab Tutorial Practical
ECTS Credits	**6**	✓ Seminar
SWL (hr/sem)	**150**	

Module Level	1	**Semester of Delivery**	1	
Administering Department	Department of Electrical Engineering Techniques	**College**	AL-Mustaqbal university/Engineering Technical College	
Module Leader	Bushra Majed Hamed	**e-mail**	bushra.majed.hamed@uomus.edu.iq	
Module Leader's Acad. Title	MSC	**Module Leader's Qualification**	.	
Module Tutor	None	**e-mail**	None	
Peer Reviewer Name	None	**e-mail**	None	
Scientific Committee Approval Date	01/09/2025	**Version Number**	1.0	

Relation with other Modules		
العلاقة مع المواد الدراسية الأخرى		
Prerequisite module	None	**Semester**	
Co-requisites module	None	**Semester**	

Module Aims, Learning Outcomes and Indicative Contents أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية	
Module Objectives أهداف المادة الدراسية	1-Training students on the basics of logical circuits used in electronic computers and how they work. 2- Building logical circuits and learning about computer operation.
Module Learning Outcomes مخرجات التعلم للمادة الدراسية	1. Learning about the different number systems. 2. Learning the arithmetic operations related to different number systems. 3. Learning the different logic gates of computer system and their work. 4. Ability to design, simplify and implement different logical and arithmetic circuits that considered the basic of digital system. 5. Ability to design, simplify and implement different sequential circuits, counters and shift registers.
Indicative Contents المحتويات الإرشادية	Indicative content includes the following: • Part 1 – Numbers Systems, Operations, and Codes Different Number Systems, Data representation (integer and fraction) using different number systems. Conversion Between Different Numbers Systems. Arithmetic operations using different number systems, and Digital Codes (BCD, Parity, Gray, etc.) [10 hrs] • Part 2- Logic Gates The Inverter (NOT Gate), AND Gate, OR Gate, NAND Gate, NOR Gate, the Exclusive-OR Gate and Exclusive-NOR Gates. [8 hrs] • Part 3 Boolean Algebra and Logic Simplification Boolean Operations and Expressions, Laws and Rules of Boolean Algebra, Simplification Using Boolean Algebra, DeMorgan's theorems,The Karnaugh Map (1, 2 , 3 and 4 variables) , SOP and POS Minimization. [8 hrs] • Part 4 Combinational Logic Analysis Basic Combinational Logic Circuits, Implementing Combinational Logic, Combinational Logic Using NAND and NOR Gates, Logic Circuit Operation with Pulse Waveform Inputs. [10 hrs] Revision problem classes [10 hrs] • Part 5 – Functions of Combinational Logic. Half , Full and Parallel Binary Adders and Subtractors. 1's and 2's Complement Subtractor, 2's Complement Adder-Subtractor, BCD Adder, etc. Comparators, Decoders, Encoders, Multiplexers, Demultiplexer [10 hrs] • Part 6- Latches, Flip-Flops, and Timers. Latches, Edge-Triggered Flip-Flops. Flip-Flop operating (R-S, T, J-K ,D) [12 hrs] • Part 7Counters Synchronous Counters, Asynchronous Counters. Design of Counters. [8 hrs] • Part 8 Shift Registers Basic Shift Register Operations: SISO, SIPO, PISO, PIPO, Bidirectional and special Types Shift Register. [6 hrs] • Revision problem classes [6 hrs] • Part 9– Microprocessor Introduction to Microprocessor: component of microprocessor, Microprocessor architecture [6 hrs]

Learning and Teaching Strategies
استراتيجيات التعلم والتعليم

Strategies	The main strategy that will be adopted in delivering this module is to encourage students' participation in the exercises, while at the same time refining and expanding their critical thinking skills. This will be achieved through classes, interactive tutorials and by considering types of simple experiments involving some sampling activities that are interesting to the students.

Student Workload (SWL)
الحمل الدراسي للطالب محسوب لـ ١٥ اسبوعا

Structured SWL (h/sem) الحمل الدراسي المنتظم للطالب خلال الفصل	93	Structured SWL (h/w) الحمل الدراسي المنتظم للطالب أسبوعيا	6.2
Unstructured SWL (h/sem) الحمل الدراسي غير المنتظم للطالب خلال الفصل	57	Unstructured SWL (h/w) الحمل الدراسي غير المنتظم للطالب أسبوعيا	3.8
Total SWL (h/sem) الحمل الدراسي الكلي للطالب خلال الفصل	150		

Module Evaluation
تقييم المادة الدراسية

		Time/Number	Weight (Marks)	Week Due	Relevant Learning Outcome
Formative assessment	Quizzes	4	10% (10)	3,5 and 10	1,3,and 4
	Assignments	7	10% (10)	2 and 12	2,3
	Projects / **Lab.**	9	10% (10)	Continuous	All
	Report	8	10% (10)	2 and 12	LO #3, #4 and #5
Summative assessment	Midterm Exam	2hr	10% (10)	8	LO #1 - #5
	Final Exam	3hr	50% (50)	15	All
Total assessment			100% (100 Marks)		

Delivery Plan (Weekly Syllabus)
المنهاج الاسبوعي النظري

	Material Covered
Week 1	Introduction - Difference between Circuit Theory and Field Theory
Week 1	• General number formula: Binary, octal, decimal and hexadecimal numbers
Week 2	• Arithmetic operations in different number system
Week 3	• complements, binary codes, BCD, Ex-3, Gray codes
Week 4	• Basic definitions, basic theorem and properties, Boolean functions
Week 5	• Canonical and Standard forms Digital Logic Gates
Week 6	• Karanough Maps: AND- OR implementation, don't care conditions
Week 7	• Subtractions, half and full adders and subtractions, binary parallel address
Week 8	• decoders, encoders, comparators
Week 9,10	• multiplexers and demultiplexers
Week 11	• Flip-flops (RS, T, D, JK …) • Master slave FF, counter • shift registers
Week 12,13	• Introduction to Microprocessor • Microprocessor architecture
Week 14	• component of microprocessor
Week 15	• Final Examination

Delivery Plan (Weekly Lab. Syllabus)
المنهاج الاسبوعي للمختبر

	Material Covered
Week 1	• Lab 1: Introduction to digital laboratory kit operation • Lab 2: Logic Gates (AND, OR, NOT, NAND, NOR).
Week 2	• Lab 3: Logic Gates (XOR, XNOR). • Lab 4: De Morgan's Theorems 1st and 2nd Laws.
Week 3	• Lab 5: Designing a combinational Logic circuit. • Lab 6: The realization of the Boolean equation.
Week 4	• Lab 9: Half Binary Subtractor. • Lab 10: Full Binary Subtractor.
Week 5	• Lab 11:Binary comparator
Week 6	• Lab 12: 2's Complement Adder- Subtractor
Week 7	• Lab 13: Flip-Flop.

Learning and Teaching Resources
مصادر التعلم والتدريس

	Text	Available in the Library?
Required Texts	Thomas L. Floyd, Digital Fundamentals, 11th Edition, Pearson Education 2015	Yes
Recommended Texts	1- Introduction to Digital Logic with Laboratory Exercises/James Feher, 2009.	No

	2- M. Morris Mano, Michael D. Ciletti, Digital Design, 5th edition, Pearson Education 2013.	
Websites	Digital Systems: From Logic Gates to Processors: https://www.coursera.org/learn/digital-systems	

<table>
<tr><td colspan="5" style="text-align:center">Grading Scheme
مخطط الدرجات</td></tr>
<tr><td>Group</td><td>Grade</td><td>التقدير</td><td>Marks %</td><td>Definition</td></tr>
<tr><td rowspan="5">Success Group (50 - 100)</td><td>A - Excellent</td><td>امتياز</td><td>90 - 100</td><td>Outstanding Performance</td></tr>
<tr><td>B - Very Good</td><td>جيد جدا</td><td>80 - 89</td><td>Above average with some errors</td></tr>
<tr><td>C - Good</td><td>جيد</td><td>70 - 79</td><td>Sound work with notable errors</td></tr>
<tr><td>D - Satisfactory</td><td>متوسط</td><td>60 - 69</td><td>Fair but with major shortcomings</td></tr>
<tr><td>E - Sufficient</td><td>مقبول</td><td>50 - 59</td><td>Work meets minimum criteria</td></tr>
<tr><td rowspan="2">Fail Group (0 – 49)</td><td>FX – Fail</td><td>راسب (قيد المعالجة)</td><td>(45-49)</td><td>More work required but credit awarded</td></tr>
<tr><td>F – Fail</td><td>راسب</td><td>(0-44)</td><td>Considerable amount of work required</td></tr>
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Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.