	Ministry of Higher Education and Scientific Research - Iraq Al-Mustaqbal University College for engineering and technology Department of Biomedical Engineering	

MODULE DESCRIPTOR FORM
نموذج وصف المادة الدراسية

Module Information معلومات المادة الدراسية					
Module Title	Digital Electronics			**Module Delivery**	
Module Type	Basic			✓ **Theory** **Lecture** ✓ **Lab** **Tutorial** **Practical** **Seminar**	
Module Code	**UOMU0101041**				
ECTS Credits	6				
SWL (hr/sem)	150				
Module Level		UGII	**Semester of Delivery**		4
Administering Department		Biomedical Engineering Dept.	**College**		College of Engineering
Module Leader			**e-mail**		
Module Leader's Acad. Title			**Module Leader's Qualification**		
Module Tutor	None		**e-mail**	None	
Peer Reviewer Name			**e-mail**		
Review Committee Approval			**Version Number**		

Relation With Other Modules العلاقة مع المواد الدراسية الأخرى			
Prerequisite module	None	**Semester**	

Co-requisites module	None	Semester	

Module Aims, Learning Outcomes and Indicative Contents
أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية

Module Aims أهداف المادة الدراسية	1. The aim of this module is to offer an introduction to the principles of digital logic to support both the design & analysis of simple digital circuits and systems and the implementation of short programs and control flows. 2. To provide the student with a strong foundation and understanding of common electronic circuits, systems, and techniques used for measurement and control in industrial environments. 3. To give the students the knowledge, competencies, and skills to analyze commonly used analog and digital systems. 4. To introduce basic combinational and sequential logic design. 5. Understand the type of number systems (decimal, binary, hexadecimal and octal) and how to convert between numbering systems. 6. Understand the arithmetic operations on the number systems. 7. An ability to describe and representation the coding system (BCD-8421, 2421 – code, Gray Code and Excess-3 Code). 8. Understand the Basic rules of Boolean algebra to simplify Boolean expressions. 9. An ability to use logic gates to construct the Sequential Logic circuit (S-R latch, D flip-flops and J-K flip-flops). 10. Understand the difference between the operations of registers and counters.
Module Learning Outcomes مخرجات التعلم للمادة الدراسية	1. Understand the operation of fundamental digital logic circuits in a variety of applications. 2. Be able to design simple combinational and sequential logic circuits using formal methods. 3. Be able to design medium scale digital systems using components from standard families and evaluate the comparative benefits of two or more design solutions. 4. Be able to employ timing diagrams in the evaluation and testing of digital systems. 5. The student understands the basic principles of number systems. 6. The student understands the basic concept and applications of combinational logic circuits. 7. The student learns how to deal with implementing and designing the

	several types of combinational logic circuits. 8. The student understands the basic concept and applications of sequential logic circuits.
Indicative Contents المحتويات الإرشادية	Indicative content includes the following. Part I: Basic Number Systems: -In this part, the binary number system and its relationship to other number systems such as decimal, hexadecimal, and octal are presented. Arithmetic operations with binary numbers are covered to provide a basis for understanding how computers and many other types of digital systems work. Also, digital codes such as binary coded decimal (BCD), the Gray code, and Excess-3 code are covered. -Numbers Signed and Arithmetic Operations with Signed Numbers: There are three forms in which signed integer numbers can be represented in binary: sign-magnitude, 1's complement, and 2's complement. Of these, the 2's complement is the most important and the sign-magnitude is the least used and then learning how signed numbers are added and subtracted. Part II: Logic Gates and Boolean algebra: The emphasis in this part is on the operation and application of logic gates (Not, OR, AND, NAND, NOR, X-OR and XNOR gate). The relationship of input and output waveforms of a gate using timing diagrams is thoroughly covered. Also covers the laws, rules, and theorems of Boolean algebra and their application to digital circuits. You will learn how to define a given circuit with a Boolean expression and then learn how to simplify logic circuits using the methods of Boolean algebra and Karnaugh map. Part III: Combinational Logic Circuit: In this part, several types of combinational logic functions are introduced including Half-Adder, Full-Adders, Parallel Binary Adders, 4-bit parallel adder, Half and Full subtractor, Adder –Subtractor, Binary-Code- Decimal (BCD) Adder, Binary Multipliers, Magnitude Comparators and Code conversion, decoders, encoders, code converters, multiplexers and demultiplexers. Part IIII: Sequential Logic Circuit: In this part, a study of the fundamentals of sequential logic circuit (S-R Latch, D Latch, D Flip-flop, J K Flip- Flop and T Flip-Flop). Also study of the applications of Flip–Flop.
Learning and Teaching Strategies استراتيجيات التعلم والتعليم	
Strategies	

	The main strategy that will be adopted in delivering this module is to encourage students' participation in the exercises, while at the same time refining and expanding their critical thinking skills. This will be achieved through classes, interactive tutorials and by considering type of simple experiments involving some sampling activities that are interesting to the students.

Student Workload (SWL)
الحمل الدراسي للطالب

Structured SWL (h/sem) الحمل الدراسي المنتظم للطالب خلال الفصل	93	**Structured SWL (h/w)** الحمل الدراسي المنتظم للطالب أسبوعيا	6
Unstructured SWL (h/sem) الحمل الدراسي غير المنتظم للطالب خلال الفصل	57	**Unstructured SWL (h/w)** الحمل الدراسي غير المنتظم للطالب أسبوعيا	4
Total SWL (h/sem) الحمل الدراسي الكلي للطالب خلال الفصل	150		

Module Evaluation
تقييم المادة الدراسية

		Time/Number	Weight (Marks)	Week Due	Relevant Learning Outcome
Formative assessment	**Quizzes**	2	10% (10)	5, 10	LO #1, 2, 10 and 11
	Assignments	2	10% (10)	2, 12	LO # 3, 4, 6 and 7
	Projects / Lab.	1	10% (10)	Continuous	
	Report	1	10% (10)	13	LO # 5, 8 and 10
Summative assessment	**Midterm Exam**	2 hr	10% (10)	7	LO # 1-7
	Final Exam	3hr	50% (50)	16	All
Total assessment			100% (100 Marks)		

Delivery Plan (Weekly Syllabus)
المنهاج الاسبوعي النظري

	Material Covered
Week 1	Introduction: digital system versus analog systems, Basic Number Systems : Type of Number Systems(decimal, binary, hexadecimal and octal).
Week 2	Conversion Between Number Systems.

Week 3	Arithmetic operations on Number Systems.
Week 4	Basic Number Systems: Coding system (BCD-8421, 2421 – code, Gray Code and Excess-3 Code).
Week 5	Signed Numbers (sign-magnitude, 1's complement, 2's complement) and Arithmetic operation with Signed Numbers
Week 6	Logic Gates and Boolean algebra: Basic Logic Gates (Not , OR, AND, NAND, NOR, X-OR and XNOR gate), Basic rules of Boolean algebra, DeMorgan's Theorems and Boolean Expression for a Logic Circuit.
Week 7	Logic Gates and Boolean algebra: Universal Property of NAND and NOR Gates, The Sum-of-Products (SOP) Form, and The Product-of-Sums (POS) Form.
Week 8	Logic Gates and Boolean algebra: Simplification of Boolean Expression (B.E) using Karnaugh map, Karnaugh map with Don't Care" Conditions and Karnaugh map POS minimization.
Week 9	Combinational Logic Circuit: Half-Adder, Full-Adders, Parallel Binary Adders, 4-bit parallel adder, Half and Full subtractor and Adder –Subtractor.
Week 10	Combinational Logic Circuit: Decoders (2x4, 3x8 and 4x16 decoder), and Decoder with Enable. Combinational Logic Implementation with Decoder.
Week 11	Combinational Logic Circuit: BCD to 7-Segment Decoder and Encoders (4x2, 8x3 and 16x4 encoder).
Week 12	Combinational Logic Circuit: Multiplexer (2x1, 4x1, 8x1 and 16x1 MUX) and Demultiplexers.
Week 13	Sequential Logic Circuit: S-R Latch, D Latch, D Flip-flop, J K Flip- Flop and T Flip-Flop.
Week 14	Registers: Serial-In Serial-Out Shift Registers, Parallel-In Parallel-Out Shift Registers, Serial-In Parallel-Out Shift Registers, Parallel-In Serial-Out Shift Registers.
Week 15	**Preparatory Week**
Week 16	**Final Exam**

Delivery Plan (Weekly Lab. Syllabus) المنهاج الاسبوعي للمختبر	
	Material Covered
Week 1	Lab 1: Verification of the truth tables of TTL gates.
Week 2	Lab 2: Verify the NAND and NOR gates as universal logic gates.
Week 3	Lab 3: Binary to Gray and Gray to Binary Cod Conversion.
Week 4	Lab 4: BCD to Excess-3 Cod Conversion
Week 5	Lab 5: Boolean laws and De-Morgan's Theorems
Week 6	Lab 6: Design and verification of the truth tables of Half and Full adder circuits.
Week 7	Lab 7: Design and verification of the truth tables of Half and Full Subtractor circuits.
Week 8	Lab 8: Verification of the truth table of the Multiplexer

Week 9	Lab 9: Verification of the truth table of the the De-Multiplexer.
Week 10	Lab 10: Verification of the truth table of the Decoder and the Encoder
Week 11	Lab 11: Design and test of an S-R flip-flop using NOR/NAND gates.
Week 12	Lab 12: Verify the truth table of a J-K flip-flop.
Week 13	Lab 13: Verify the truth table of a D flip-flop.
Week 14	Lab 14: Design of 4-bit shift register
Week 15	**Final Exam**

Learning and Teaching Resources مصادر التعلم والتدريس		
	Text	**Available in the Library?**
Required Texts	Fundamentals of Electric Circuits, C.K. Alexander and M.N.O Sadiku, McGraw-Hill Education	Yes
Recommended Texts	DC Electrical Circuit Analysis: A Practical Approach Copyright Year: 2020, dissidents.	No
Websites	https://www.coursera.org/browse/physical-science-and-engineering/electrical-engineering	

APPENDIX:

GRADING SCHEME مخطط الدرجات				
Group	**Grade**	التقدير	**Marks (%)**	**Definition**
Success Group (50 - 100)	**A** - Excellent	امتياز	90 - 100	Outstanding Performance
	B - Very Good	جيد جدا	80 - 89	Above average with some errors
	C - Good	جيد	70 - 79	Sound work with notable errors
	D - Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	E - Sufficient	مقبول	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	**FX** – Fail	مقبول بقرار	(45-49)	More work required but credit awarded
	F – Fail	راسب	(0-44)	Considerable amount of work required
Note:				

NB Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.