MODULE DESCRIPTION FORM

نموذج وصف المادة الدراسية

Module Information معلومات المادة الدراسية					
Module Title	**Digital Electronics**			**Module Delivery**	
Module Type				☒ **Theory** ☒ **Lecture** ☒ **Lab** ☐ **Tutorial** ☐ **Practical** ☐ **Seminar**	
Module Code	**UOMU031011**				
ECTS Credits	**6.00**				
SWL (hr/sem)	**150**				
Module Level	UGII		**Semester of Delivery**	4	
Administering Department	PHY		**College**	COS	
Module Leader	Rusul Abdul ameer Ghazi		**e-mail**		
Module Leader's Acad. Title	Asst.Professor		**Module Leader's Qualification**	Ph.D.	
Module Tutor	Name (if available)		**e-mail**	E-mail	
Peer Reviewer Name	Name		**e-mail**	E-mail	
Scientific Committee Approval Date	15/10/2025		**Version Number**	1.0	

Relation with other Modules العلاقة مع المواد الدراسية الأخرى			
Prerequisite module	None	**Semester**	
Co-requisites module	None	**Semester**	

Module Aims, Learning Outcomes and Indicative Contents أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية	
Module Objectives أهداف المادة الدراسية	To understand the following subjects: 1. Number systems and codes in digital electronics 2. Introduce the basic elements of digital circuits. 3. Basic Logic Gates 4. Combinational circuit. 5. Boolean Expression and Boolean Algebra. 6. Applied logic circuits. 7. Adders and Subtractors circuits 8. Sequential circuit 9. Flip Flop Basics – Types, Truth Table, Circuit, and Applications. 10. Shift Register, parallel and serial. 11. Analog-to-Digital circuits. 12. Digital-to-Analog circuits. 13. Digital counter circuits, Up counters. Down counters. Frequency division. 14. Basic memory circuits.
Module Learning Outcomes مخرجات التعلم للمادة الدراسية	1.To acquire the basic knowledge of digital logic levels and application of knowledge to understand digital electronics circuits. 2.To prepare students to perform the analysis and design of various digital electronic circuits. 3.To introduce the basic concepts and laws involved in the Boolean algebra and logic families and digital circuits. 4.To familiarize with the different number systems, logic gates, and combinational and sequential circuits utilized in the different digital circuits and systems. Provide ability to design and analysis of the digital circuit and system. Understand the basic software tools for the design and implementation of digital circuits and systems. Reinforce theory and techniques taught in the classroom through experiments and projects in the laboratory. 5.To understand the working principle of data processing circuits, arithmetic circuits, and sequential circuits. 6.Students will get an overview of microprocessor architecture and programming.
Indicative Contents المحتويات الإرشادية	Indicative content includes the following. Numbers systems, Binary numbers, Boolean algebra, Boolean minimisation, Combinational circuits, Logic families, flip flops Counters, Multivariable Boolean

	reduction, Synchronous and asynchronous sequential circuits, Programmable logic design techniques Logic Gates RTL, DTL, TTL, ECL, ICL, HTL, NMOS & CMOS logic gates, Circuit diagram and analysis characteristics and specifications, tri-state gates. Combinational Circuits Problem formulation and design of combinational circuits, Adder / Subtractor, Encoder / decoder, Mux/Demux, Code-converters, Comparators, Implementation of combinational logic using standard ICs, ROM, EPROM, EEPROM, PAL, PLA and their use in combinational circuit design. Sequential Circuits Flipflops - SR, JK, T, D, Master/Slave FF, Triggering of FF, Analysis of clocked sequential circuits - their design, State minimization, state assignment, Circuit implementation, Registers-Shift registers, Ripple counters, Synchronous counters, Timing signal, RAM, Memory decoding, Semiconductor memories. Fundamental Mode Sequential Circuits Stable, Unstable states, Output specifications, Cycles and Races, Racefree Assignments, Hazards, Essential hazards, Pulse mode sequential circuits.

Learning and Teaching Strategies استراتيجيات التعلم والتعليم	
Strategies	This module will be presented to the students through a series of lectures, tutorials, practicals and investigations. Learning materials will include lecture notes and technical demonstrations. It is preferred that students study both analogue and digital elements in parallel. Throughout the course, so that students are exposed to the differences and similarities in both fields and are able to better reflect on their experiences. Extensive use will be made of to supplement learning materials and provide quizzes and exams for the assessment. A 2-hour lecture will be provided weekly. The material for the weekly lecture will be made available beforehand, to allow students to prepare as necessary. Where relevant, further reading will be made available post-lecture. A 2-hour lab session will be provided weekly. The intent is for the student to put into practice the theory gained during the weekly lecture.

Student Workload (SWL) الحمل الدراسي للطالب محسوب لـ ١٥ اسبوعا			
Structured SWL (h/sem) الحمل الدراسي المنتظم للطالب خلال الفصل	88	**Structured SWL (h/w)** الحمل الدراسي المنتظم للطالب أسبوعيا	6
Unstructured SWL (h/sem) الحمل الدراسي غير المنتظم للطالب خلال الفصل	62	**Unstructured SWL (h/w)** الحمل الدراسي غير المنتظم للطالب أسبوعيا	4
Total SWL (h/sem) الحمل الدراسي الكلي للطالب خلال الفصل	**150**		

Module Evaluation تقييم المادة الدراسية					
		Time/Number	**Weight (Marks)**	**Week Due**	**Relevant Learning Outcome**
Formative assessment	**Quizzes**	2	10% (10)	5 and 10	LO #1, #2 and #10, #11
	Assignments	2	10% (10)	2 and 12	LO #3, #4 and #6, #7
	Projects / Lab.	1	10% (10)	Continuous	All
	Report	1	10% (10)	13	LO #5, #8 and #10
Summative assessment	**Midterm Exam**	2hr	10% (10)	7	LO #1 - #7
	Final Exam	3hr	50% (50)	16	All
Total assessment			100% (100 Marks)		

Delivery Plan (Weekly Syllabus) المنهاج الاسبوعي النظري	
	Material Covered
Week 1	Number Systems and Codes
Week 2	Seven Basic Logic Gates
Week 3	Combinatorial Logic
Week 4	Boolean Algebra, De M organ's Theorem
Week 5	Arithmetic Operations and Circuits, Half Adder and Full Adder
Week 6	Flip-Flops and Registers. a.S-R Flip-Flop b. D Flip-Flop c. J-K Flip-Flop
Week 7	Counter Circuits: a. Asynchronous Counters b. Synchronous Counters
Week 8	Shift Registers: Serial/Parallel Data Conversions.
Week 9	**Mid exam.**
Week 10	Analog-to-Digital circuits
Week 11	Digital-to-Analog circuits
Week 12	Multivibrators: Astable
Week 13	Multivibrators: Monostable
Week 14	Schmitt Trigger
Week 15	**Exam.**
Week 16	**Revision for final exam**

Delivery Plan (Weekly Lab. Syllabus) المنهاج الاسبوعي للمختبر	
	Material Covered
Week 1	Lab 1: TTL ICs
Week 2	Lab 2: Breadboards and Building Digital Circuits. AND, OR and NOT Gates
Week 3	Lab 3: Basic Combinational Logic & Gates with Many Inputs
Week 4	Lab 4: DeMorgan's Theorem
Week 5	Lab 5: Half and full adder circuit, SN7486, SN7483
Week 6	Lab 6: Flip Flop circuit
Week 7	Lab 7: Universal Shift register SN74194.

Learning and Teaching Resources مصادر التعلم والتدريس		
	Text	**Available in the Library?**
Required Texts	Textbooks: Fundamentals of Digital Electronics, Natarajan, 1st Edition (2020) Suggested references: Digital Circuits Logic and Design, Ronald C. Emery, 1st Edition (2016)	No
Recommended Texts	M. Morris Mano, Michael D. Ciletti, "Digital Design", Prentice Hall of India Pvt. Ltd., 2008. Brian Holdsworth, Clive Woods, "Digital Logic Design", Elsevier India Pvt. Ltd., 2005. Samir Palnitkar, "Verilog HDL, A Guide to Digital Design and Synthesis", Prentice Hall of India Pvt. Ltd., 2005.	No
Websites	https://byjus.com/physics/digital-electronics/	

Grading Scheme مخطط الدرجات				
Group	**Grade**	التقدير	**Marks %**	**Definition**
Success Group (50 - 100)	**A -** Excellent	امتياز	90 - 100	Outstanding Performance
	B - Very Good	جيد جدا	80 - 89	Above average with some errors
	C - Good	جيد	70 - 79	Sound work with notable errors
	D - Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	E - Sufficient	مقبول	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	**FX –** Fail	راسب (قيد المعالجة)	(45-49)	More work required but credit awarded
	F – Fail	راسب	(0-44)	Considerable amount of work required

Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.