MODULE DESCRIPTION FORM

نموذج وصف المادة الدراسية

Module Information معلومات المادة الدراسية					
Module Title	**Digital Logic**			**Module Delivery**	
Module Type	**Core**			☒**Theory** ☐**Lecture** ☒**Lab** ☐**Tutorial** ☐**Practical** ☐**Seminar**	
Module Code	**UOMU0207021**				
ECTS Credits	**7**				
SWL (hr/sem)	**175**				
Module Level		UGI	**Semester of Delivery**		2
Administering Department			**College**	NETC	
Module Leader	Noor AbdAlKarem Mohammedali		**e-mail**	noor.abdulkareem@uomus.edu.iq	
Module Leader's Acad. Title		Lecturer	**Module Leader's Qualification**		PhD
Module Tutor	Name (if available)		**e-mail**	E-mail	
Peer Reviewer Name					
Scientific Committee Approval Date		01/10/2024	**Version Number**		1.0

Relation with other Modules العلاقة مع المواد الدراسية الأخرى			
Prerequisite module	None	**Semester**	
Co-requisites module	None	**Semester**	

Module Aims, Learning Outcomes and Indicative Contents أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية	
Module Objectives أهداف المادة الدراسية	This course aims to enable the student to: 1. Explain the number systems. 2. Perform arithmetic operations on binary number systems. 3. Define the logic gates. 4. Write the logic expression of the logic circuits. 5. Produce the truth table for the logic expressions. 6. Simplify the Boolean expressions. 7. Understand the functions of combinational logic circuits. 8. Analyze and design various combinational logic circuits.
Module Learning Outcomes مخرجات التعلم للمادة الدراسية	1. Represent any given number in different bases (such as bases 2, 8, and 16). 2. Implement the arithmetic operations on binary numbers. 3. Obtain the 1's complement and 2's complement of binary numbers. 4. Identify the logic gates by their logic symbol, write the logic expression, and produce the truth table for the logic gates. 5. Analyze a logic circuit to determine its logic expression and truth table. 6. Employ theorems of Boolean algebra to simplify logic expressions. 7. Determine the standard SOP expression and standard POS expression from the truth table. 8. Use a Karnaugh map to minimize POS & SOP expressions. 9. Convert nonstandard logic expressions to standard logic expressions. 10. Implement the logic functions using only NAND gates or only NOR gates. 11. Design of various combinational logic circuits such as adders, subtractors, comparators, and code converters.
Indicative Contents المحتويات الإرشادية	<u>Part A - Number Systems</u> Define number systems, convert a decimal number to any radix number, convert a binary number to an octal or hexadecimal number and vice versa, and convert an octal number to a hexadecimal number and vice versa. [1-3 weeks] <u>Part B - Arithmetic operations & logic gates</u> Perform arithmetic operations on binary numbers, convert a binary number to its 1's complement, and 2's complement, Identify the logic gates, write the logic expression, and produce the truth table. [1-2 weeks] <u>Part C - Combinational logic circuit</u> Analyze a combinational logic circuit, draw a logic diagram, theorems of Boolean algebra, DE Morgan's theorem, standard SOP & POS expressions, use a Karnaugh map to minimize POS & SOP expressions, convert nonstandard expressions to standard expressions, implement the logic expressions using only NAND gates or only NOR gates. [1-5 weeks] <u>Part D - Design combinational logic circuits</u> • Arithmetic logic circuits: half-adder and full-adder logic circuits, half-subtractor and full-subtractor logic circuits. [1-2 weeks]

	• Code converters logic circuits: binary to gray code converter circuit and vice versa, Binary-to-BCD Code circuit, BCD to Excess-3 code converter circuit and vice versa. [1-2 weeks] • Comparators logic circuits: 1-bit & 2-bit comparators logic circuits. [1 week]

Learning and Teaching Strategies استراتيجيات التعلم والتعليم	
Strategies	• Interactive lecturing style, with opportunities for questions. • Encourage students' participation in the exercises, while at the same time refining and expanding their critical thinking skills. • Interactive simulation for the logic circuits. • Make tutorial questions for formative feedback. • Assessments related to students' answers are delivered with scientific comments.

Student Workload (SWL) الحمل الدراسي للطالب محسوب لـ ١٥ اسبوعا			
Structured SWL (h/sem) الحمل الدراسي المنتظم للطالب خلال الفصل	93	**Structured SWL (h/w)** الحمل الدراسي المنتظم للطالب أسبوعيا	6.2
Unstructured SWL (h/sem) الحمل الدراسي غير المنتظم للطالب خلال الفصل	82	**Unstructured SWL (h/w)** الحمل الدراسي غير المنتظم للطالب أسبوعيا	5.5
Total SWL (h/sem) الحمل الدراسي الكلي للطالب خلال الفصل	**175**		

Module Evaluation تقييم المادة الدراسية					
		Time/Number	**Weight (Marks)**	**Week Due**	**Relevant Learning Outcome**
Formative assessment	**Quizzes**	2	10% (10)	4 and 10	L #2, #3 and #9, #8
	Assignments	2	10% (10)	7 and 15	L #6, #7 and #13, #14
	Projects / Lab.	1	10% (10)	Continuous	All
	Report	1	10% (10)	12	LO #5, #10 and #12
Summative assessment	**Midterm Exam**	2hr	10% (10)	8	LO #1 - #7
	Final Exam	3hr	50% (50)	16	All
Total assessment			100% (100 Marks)		

Delivery Plan (Weekly Syllabus) المنهاج الاسبوعي النظري	
	Material Covered
Week 1	Introduction - Number Systems: binary, decimal, octal, and hexadecimal numbers.
Week 2	Convert a decimal number to any radix number.
Week 3	Convert a binary number to an octal or hexadecimal number and vice versa, and convert an octal number to a hexadecimal number and vice versa.
Week 4	Perform arithmetic operations on binary numbers, and convert a binary number to its 1's complement, and 2's complement.
Week 5	Identify the logic gates, write the logic expression, and produce the truth table.
Week 6	Analyze a combinational logic circuit, draw a logic diagram, and theorems of Boolean algebra.
Week 7	DE Morgan's theorem, standard SOP expression, and standard POS expression.
Week 8	Mid-term Exam + Construct a Karnaugh map for two, three, and four variables, use a Karnaugh map to minimize POS & SOP expressions.
Week 9	Convert nonstandard expressions to standard expressions, and Use the Karnaugh map to convert between POS and SOP.
Week 10	Use NAND gates to create other logic gates, Use NOR gates to create other logic gates, and implement the logic functions using only NAND gates or only NOR gates.
Week 11	Design half-adder & full-adder logic circuits, and use full-adders to implement a parallel binary adder.
Week 12	Design the half- subtractor & full-subtractor logic circuits, and use full-subtractors to implement a parallel binary subtractor.
Week 13	Explain the concept of code converters, and describe gray code, BCD, and excess-3 code.
Week 14	Design combinational logic circuits that convert from one coding method to another.
Week 15	Design 1-bit, and 2-bit comparators using logic gates, and use the 74HC85 comparator to compare the magnitudes of two 4-bit numbers.
Week 16	**Final Exam.**

Delivery Plan (Weekly Lab. Syllabus) المنهاج الاسبوعي للمختبر	
	Material Covered
Week 1	Lab 1: Explain the function of a logic gates (AND, OR, NOT, AND, NOR, XOR , and XNOR) using the logical board.
Week 2	Lab 2: Implement the logic gates (AND, OR, & NOT) using diodes, transistors, and resistors.

Week 3	Lab 3: Verify the truth table of logic gates (AND, OR, NOT, NAND, NOR, XOR, &XNOR) by using integrated circuits IC (7408, 7432, 7404, 7400, 7402, & 7486).
Week 4	Lab 4: Boolean's algebraic
Week 5	Lab 5: DE Morgan's theorem.
Week 6	Lab 6: Implement logic gates (AND, OR, NOT, NAND, NOR, XOR & XNOR) using NAND gates only.
Week 7	Lab 7: Implement logic gates (AND, OR, NOT, NAND, NOR, XOR & XNOR) using NOR gates only.
Week 8	Lab 8: Design the half-adder circuit using logic gates.
Week 9	Lab 9: Design the full-adder circuit using logic gates.
Week 10	Lab 10: Design the half-subtractor circuit using logic gates.
Week 11	Lab 11: Design the full-subtractor circuit using logic gates.
Week 12	Lab 12: Design the full subtractor circuit using logic gates.
Week 13	Lab 13: Implement a binary to gray code converter circuit using logic gates.
Week 14	Lab 14: Implement the BCD to Excess-3 code converter circuit using logic gates.
Week 15	Lab 15: Design (1-bit) comparator circuit using logic gates.

Learning and Teaching Resources
مصادر التعلم والتدريس

	Text	Available in the Library?
Required Texts	1. G. K. Kharate, "Digital Electronics" Oxford university press, 7th edition, ISBN 13: 978-0-19-806183-0, 2013. 2. Thomas L. Floyd, "Digital Fundamentals" Pearson Education, 11th edition, ISBN 10: 1-292-07598-8, 2015. 3. T. Ndjountche "Digital Electronics 1", John Wiley & Sons, 1st edition, ISBN 978-1-84821-984-7, 2016. 4. N. S. Widmer, G. L. Moss, R. J. Tocci, "Digital Systems", Pearson Education Limited e, 12th edition, ISBN 978-0-134-22013-0, 2017. 5. Shuqin Lou, Chunling Yang, "Digital Electronic Circuits" Science Press, 4th edition, ISBN 978-3-11-061466-4, 2019.	NO Yes Yes Yes NO
Recommended Texts	1. A.P. Godse and D.A. Godse, "Digital Logic Circuits" Technical Publications Pune, 4th edition, ISBN: 9788184316506, 2009. 2. R. S. Sedha, "A TEXTBOOK OF DIGITAL ELECTRONICS" S. Chand & Company ltd, ISBN: 81-219-2378-6, 2010. 3. D. P. leach and a. p. malvino, "digital principles and applications", tata mcgraw hill education,7th edition, ISBN:978-0-07-014170-4, 2011. 4. D. P. Kothari, and J. S. Dhillon "digital circuits and design" Pearson education, ISBN 978-93-325-4353-9, 2015. 5.S. Salivahanan and S. Arivazhagan, "DIGITAL CIRCUITS AND DESIGN" Oxford university press, 5th edition, ISBN-13 : 978-0199488681, 2018.	NO Yes Yes No NO
Websites	https://www.allaboutcircuits.com/textbook/digital/	

Grading Scheme مخطط الدرجات				
Group	**Grade**	التقدير	**Marks %**	**Definition**
Success Group (50 - 100)	**A -** Excellent	امتياز	90 - 100	Outstanding Performance
	B - Very Good	جيد جدا	80 - 89	Above average with some errors
	C - Good	جيد	70 - 79	Sound work with notable errors
	D - Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	E - Sufficient	مقبول	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	**FX –** Fail	راسب (قيد المعالجة)	(45-49)	More work required but credit awarded
	F – Fail	راسب	(0-44)	Considerable amount of work required

Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.